A Pipelined Loop-Unrolled SAR ADC with Open-Loop Amplification

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DEPARTMENT OF ELECTRICAL AND INFORMATION TECHNOLOGY
FACULTY OF ENGINEERING | LTH | LUND UNIVERSITY

A Pipelined Loop-Unrolled SAR ADC with Open-Loop Amplification

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December 2, 2025

Printed in Sweden
Tryckeriet i E-huset, Lund

Abstract

This thesis presents the analysis and design of a three-stage pipelined loop-unrolled successive approximation register (Lu-SAR) analog-to-digital converter (ADC) implemented in 65 nm CMOS technology. The ADC is designed to achieve high speed and good linearity under low supply voltage and limited power, targeting wireless communication and high-speed data acquisition applications.

At the system level, inter-stage redundancy is used. The main non-idealities, including sampling distortion, comparator offset, capacitor mismatch, and open-loop amplifier nonlinearity, are analyzed and modeled. Open-loop residue amplifiers are adopted to improve speed and power efficiency, while digital background calibration is used to correct their gain and nonlinearity errors.

A least-mean-square (LMS) based digital background calibration algorithm is developed to correct gain error, bit-weight deviation, and amplifier nonlinearity. Simulation results at both the behavioral and circuit level show that the proposed calibration can effectively restore the linearity. After calibration, the ADC achieves more than 60 dB SNDR and over 80 dB SFDR at 300 MS/s, which confirms the effectiveness of the proposed architecture and calibration scheme.

Popular Science Summary

Human civilization has always moved forward with new inventions. From the steam engines of the first industrial revolution to the spread of electricity, from the birth of computers to the rise of artificial intelligence (AI), each wave of innovation has changed how people understand and shape the world.

As technology developed, the way we handle information also changed from continuous analog signals, like sound or temperature, to digital signals made of zeros and ones. Together, these two types of signals form the foundation of the modern information world.

Today, AI is entering every corner of life: smart factories, self-driving cars, and medical devices all rely on collecting and understanding large amounts of data. To make this possible, we need a bridge between the real world and the digital world. This bridge is the analog-to-digital converter (ADC), a tiny but essential circuit that turns natural signals into numbers computers can understand.

This thesis explores a new ADC design that combines speed, accuracy, and low power. It also introduces a learning algorithm that helps the circuit automatically correct small internal errors.

By making this key interface more efficient and reliable, the work contributes to the technology that allows AI systems to sense and respond to the world more precisely and intelligently.

Acknowledgments

I would like to express my sincere gratitude to Wenbo Li for his continuous guidance throughout this thesis. He helped me understand the system level design of the ADC and the operating principles of each circuit block. I also thank him for his guidance on my short paper about the comparator offset calibration, where his advice and detailed feedback played an important role in shaping the work. I would also like to thank Pietro Andreani for the discussions related to that short paper and for his valuable comments and suggestions, which helped improve the quality of the work. I am grateful to my formal supervisor Sijia Cheng. She helped me with all the administrative procedures related to the thesis.

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Chapter 1

Introduction

1.1 Background and Motivation

With the development of wireless communication, baseband Analog-to-digital Converters(ADCs) must operate at higher sampling rates while maintaining high resolution. At the same time, power efficiency has become a critical design target, especially for portable and battery-powered wireless devices. These conflicting requirements of high speed, high accuracy, and low power make the design of high-performance ADCs increasingly challenging.

Furthermore, process scaling in modern CMOS technologies brings both opportunities and difficulties. While smaller device dimensions allow faster operation and lower supply voltages, they also lead to smaller intrinsic gain and higher component mismatch, which can degrade ADC performance.[1] Therefore, it is important to explore circuit techniques and design methodologies that can achieve high linearity and precision under limited voltage headroom and power budget.

The motivation of this work is to develop a high-speed, high-resolution ADC suitable for wireless communication, where both power efficiency and linearity are critical.

1.2 ADC basics

Baseband ADCs convert analog signals, which are down-converted by RF front-end circuits, into digital codes. The resolution and sampling rate of ADCs directly affect the signal-to-noise ratio(SNR) and bandwidth of wireless communication systems.

The main ADC architectures include Delta-Sigma, Successive Approximation (SAR), Flash, Pipeline, and Single-Slope types. Among them, Pipeline and SAR ADCs are most commonly used in wireless systems. Pipeline ADCs are often used in broadband receivers, as the pipeline structure allows higher speed. SAR ADCs perform quantization through a binary search algorithm, and are typically used in applications that require low power consumption. [2]

1.2.1 SAR ADC

SAR ADCs have gained a lot of benefits from the improvement of technology nodes, because many parts of SAR ADCs are digital and can scale well with technology. ADC architectures based on SAR, such as Time-interleaved(TI)-SAR and pipelined-SAR, have also received a lot of attention [3–6]. A SAR ADC mainly consists of a DAC, a comparator, and the necessary digital logic, as illustrated as Figure 1.1. Its working flow is very similar to a binary search. Assuming the ADC's

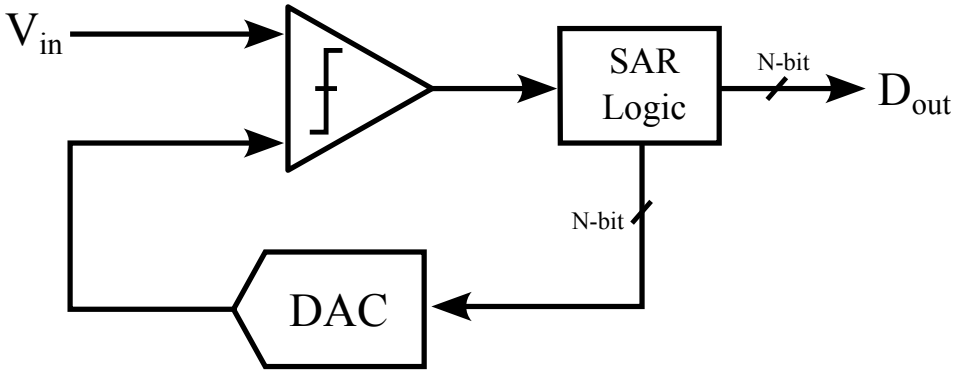


Figure 1.1: Simplifed Schematic of SAR ADCs

input range is from $-V_{ref}$ to V_{ref}, and the input voltage is V_{in}, after sampling, the DAC initially outputs 0. The comparator then compares V_{in} with the DAC output. If the input voltage is greater than the DAC output, the most significant bit (MSB) of the SAR register is set to 1; otherwise, it remains 0. The DAC output is then updated according to the current SAR code. If the current SAR code is 0, the DAC outputs $-V_{ref}/2$; otherwise, it outputs $V_{ref}/2$. This comparison and update process repeats itself from the MSB to the least significant bit (LSB)[7].

1.2.2 Pipeline ADC

Figure 1.2 shows a typical pipeline ADC. The conversion proceeds as follows: the input signal V_{IN} is first sampled and held, then sent to the first-stage sub-ADC, and generates the first digital output. This digital code is converted back to analog through the sub-DAC inside the multiplying DAC (MDAC), and subtracted from the original input to obtain the residue voltage. The residue amplifier then amplifies the residue to generate $V_{\mathrm{RES},1}$, which is sampled and held by the next stage for subsequent quantization. Each subsequent stage repeats this process until the final stage generates the least significant bits.[7]

Typically, pipeline ADC employs flash ADC as a sub ADC, which can achieve high conversion speed. The comparators in a flash ADC operate at the same time, which leads to high power consumption. A single flash ADC has limited resolution, so multiple stages are cascaded to achieve higher overall precision. Increasing the number of stages increases the number of residue amplifiers, which are generally power-hungry and thus contribute significantly to the total power consumption. In addition, the accuracy of a pipeline ADC is strongly affected

by the gain error and nonlinearity of the residue amplifier. Conventional closed-loop amplifiers require high open-loop gain to ensure accurate closed-loop gain. Traditional closed-loop op-amp architectures are reaching their performance limits, leading to high design complexity and large power consumption in high-speed, high-resolution applications.

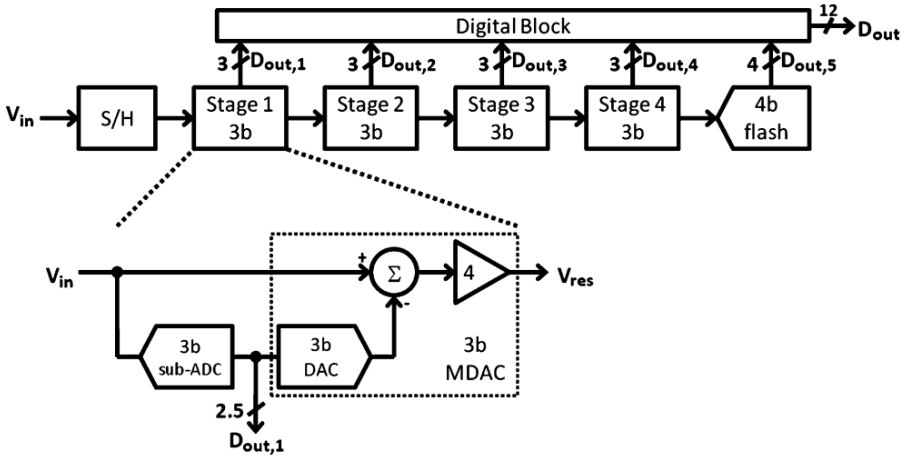


Figure 1.2: Simplified Schematic of a 12-bit Pipeline ADC[8]

1.3 Performance Metrics of ADCs

The performance metrics of ADCs are described in [7]. For convenience of reference, we briefly restate the relevant definitions here.

The performance of an analog-to-digital converter (ADC) is usually evaluated by several static and dynamic metrics. The static metrics describe the accuracy of the transfer function, while the dynamic metrics describe the converter behavior under sinusoidal input signals.

1.3.1 Static performance

The most common static performance metrics are the differential nonlinearity (DNL) and the integral nonlinearity (INL). DNL measures the deviation of each code width from the ideal value of 1 LSB. It reflects whether the output codes are uniformly spaced. DNL can be expressed as

$$\mathrm{DNL}[i] = \frac{V_{i+1} - V_i}{V_{\mathrm{LSB,ideal}}} - 1, \tag{1.1}$$

where V_i is the input threshold corresponding to code i, and $V_{\mathrm{LSB,ideal}}$ is the ideal voltage step size. A DNL larger than -1 LSB ensures the ADC is monotonic and does not miss any code.

INL represents the accumulated deviation of the actual transfer curve from the ideal straight line. It indicates the overall linearity of the converter. INL is usually calculated as

$$\mathrm{INL}[i] = \frac{V_i - i \cdot V_{\mathrm{LSB,ideal}}}{V_{\mathrm{LSB,ideal}}}. \tag{1.2}$$

Smaller INL means the converter transfer curve is closer to the ideal linear relation between input voltage and output code.

1.3.2 Dynamic performance

Dynamic metrics are obtained by applying a sinusoidal input and analyzing the digital output spectrum. The main parameters include the signal-to-noise-and-distortion ratio (SNDR), effective number of bits (ENOB), and spurious-free dynamic range (SFDR).

SNDR is defined as the ratio of the power of the fundamental signal to the total power of noise and distortion components:

$$\mathrm{SNDR} = 10 \log_{10} \left(\frac{P_{\mathrm{signal}}}{P_{\mathrm{noise}} + P_{\mathrm{distortion}}} \right). \tag{1.3}$$

The ENOB is derived from the SNDR and represents the equivalent resolution of the ADC, given by

$$\mathrm{ENOB} = \frac{\mathrm{SNDR} - 1.76}{6.02}. \tag{1.4}$$

For an ideal N-bit ADC, the theoretical SNDR is $6.02N + 1.76$ dB.

SFDR is the ratio between the power of the fundamental signal and the largest spurious component in the output spectrum:

$$\mathrm{SFDR} = 10 \log_{10} \left(\frac{P_{\mathrm{signal}}}{P_{\mathrm{spur,max}}} \right). \tag{1.5}$$

1.4 Outline of this Thesis

This thesis is organized into six chapters.

Chapter 1 introduces the background and motivation of this work, followed by a brief overview of the fundamentals of ADC operation and the main performance metrics used to evaluate ADCs.

Chapter 2 presents the system-level analysis of the proposed ADC. The working principle of the loop-unrolled SAR ADC is first reviewed, followed by the overall system design and performance trade-offs. The main nonlinearity sources and noise are analyzed and modeled at the behavioral level.

Chapter 3 describes the detailed circuit design of the proposed ADC. The design and operation of the loop-unrolled SAR sub-ADCs and the open-loop residue amplifiers are introduced, along with key implementation considerations.

Chapter 4 focuses on the calibration methods. A background calibration technique based on the LMS algorithm is discussed for bit-weight, amplification gain, and nonlinearity, A foreground calibration method is presented for comparator offset.

Chapter 5 presents the simulation results of the proposed ADC, including dynamic performance under different input amplitudes, input frequency, and different process corners.

Finally, Chapter 6 summarizes this work and discusses possible directions for future research and improvement.

Chapter 2

System Level Analysis

2.1 Fundamentals of Loop-Unrolled SAR ADC

A simplified diagram of the loop-unrolled SAR (Lu-SAR) ADC is shown in Figure 2.1. In an N-bit Lu-SAR converter, N comparators are used, and each comparator is responsible for one bit decision. The conversion starts with sampling and holding the input. After sampling, the first comparator performs its comparison. Once this comparison finishes, its output directly initiates the CDAC switching and settling, without passing through additional flip-flop logic as in a conventional SAR [5]. After the CDAC settles for a proper amount of time, the next comparator is activated. This asynchronous sequence continues until all bits are resolved. Because all comparators are reset during the sampling phase, the overall conversion speed is not limited by comparator reset time.

Compared with a traditional SAR ADC that relies on a single comparator for all comparisons, the Lu-SAR structure uses multiple comparators. Each comparator carries its own offset, and these offsets appear at different bit positions. As a result, the quantization thresholds are shifted in a non-uniform way, which introduces distortion in the output.[9]

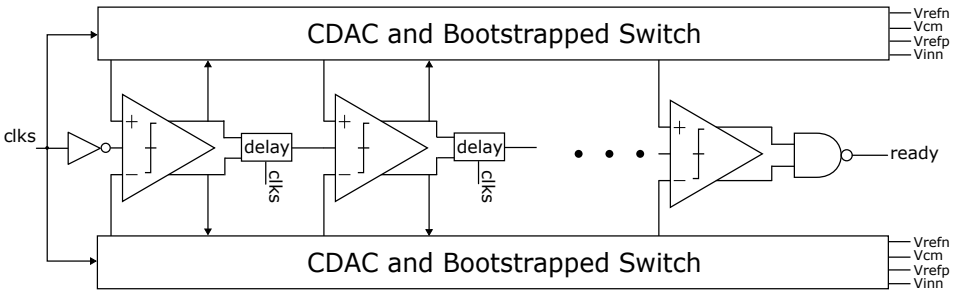


Figure 2.1: Schematic of Loop-Unrolled SAR ADC[9]

2.2 Inter-Stage Redundancy in Pipeline ADCs

In a pipeline ADC, each stage can be viewed as a mapping function:

$$f_i : V_{in,i} \mapsto (D_i, V_{res,i}), \tag{2.1}$$

where D_i is the digital output of the sub-ADC and $V_{res,i}$ is the residue passed to the next stage.

According to the invertibility principle in [10], for a system S, if two distinct input cannot lead to the same output(injective), then S is inversible.

In our case, if every f_i is injective within its input range, the overall composite mapping

$$V_{out} = f_N \circ f_{N-1} \circ \cdots \circ f_1(V_{in}) \tag{2.2}$$

remains invertible, and the original input can be reconstructed by the digital back-end as

$$V_{in} = \sum_{i=1}^{N} \frac{V_{LSB,i} D_i + Q_{n,i}}{\prod_{j=1}^{i-1} A_j}, \tag{2.3}$$

where $Q_{n,i}$ represents the quantization noise of stage i.

In the ideal case, each sub-ADC makes the correct decision, and the residue satisfies $|V_{res,i}| \leq 0.5\ V_{LSB,i}$, so after amplification, the residue remains within the input range of the next stage, preserving the one-to-one mapping.

However, in practical implementations, comparator offsets, incomplete CDAC settling, or other errors may lead to an incorrect decision:

$$|V_{res,i}^{\text{error}}| = |V_{in,i} - D_{i,\text{error}} V_{LSB,i}| > 0.5\ LSB \tag{2.4}$$

and after amplification,

$$|V_{amp,i}| = |A_i V_{res,i}^{\text{error}}| \tag{2.5}$$

If $|V_{amp,i}|$ exceeds the valid input range of the next sub-ADC, multiple residue values are mapped to the same output code due to output saturation of the quantizer. This effectively collapses the mapping f_i, destroying its injectivity and causing irreversible information loss.

To prevent this, inter-stage redundancy is introduced. By reducing the inter-stage gain, the amplified residue is constrained within the acceptable range:

$$|A_i V_{res,i}| \leq \frac{V_{FS}}{2} \tag{2.6}$$

With 1-bit redundancy, the allowable residue range expands from ±0.5 LSB to ±1 LSB, enabling the next stage to tolerate small decision or gain errors from the previous stage without violating the valid input region.

From a system viewpoint, redundancy ensures that each f_i remains locally injective even in the presence of small nonidealities, preserving the reversibility of the overall ADC mapping. Thus, the essence of inter-stage redundancy is not to directly correct quantization errors, but to guarantee information preservation by maintaining the invertibility of the pipeline.

2.3 Top Level Design

In this design, the ADC is implemented in 65 nm CMOS technology with a target sampling rate of 300 MS/s and a linearity higher than 70 dB. Considering the trade-offs among speed, resolution, and power consumption, a three-stage pipelined SAR (pipe-SAR) architecture is chosen. Compared with the conventional pipeline flash architecture, the power consumption of the pipe-SAR structure is much lower. On the other hand, compared with the two-stage pipe-SAR structure, the three-stage architecture can achieve higher speed under 65 nm technology, since it is difficult for a two-stage pipe-SAR to reach 300 MS/s due to the time limitation of each stage.

In the three-stage pipe-SAR architecture, the time budget of each stage consists of sampling, quantization, and residue amplification. The first stage includes the sampling time, the quantization time of the first SAR ADC, and the amplification time of the first residue amplifier:

$$t_{\text{stage1}} = t_{\text{smp,1}} + t_{\text{q,1}} + t_{\text{amp,1}\to 2} \tag{2.7}$$

The second stage includes the amplification time from the first residue amplifier, the quantization time of the second SAR ADC, and the amplification time of the second residue amplifier:

$$t_{\text{stage2}} = t_{\text{amp,1}\to 2} + t_{\text{q,2}} + t_{\text{amp,2}\to 3} \tag{2.8}$$

The third stage includes the amplification time from the second residue amplifier and the quantization time of the last SAR ADC:

$$t_{\text{stage3}} = t_{\text{amp,2}\to 3} + t_{\text{q,3}} \tag{2.9}$$

Since the sampling and residue amplification in the first stage require higher precision, the timing bottleneck mainly comes from the first stage, while the second stage is slightly more relaxed, and the third stage is the most relaxed. Based on these timing considerations, fewer bits are assigned to the first two stages. An initial configuration of 3-3-6 bits is analyzed. To tolerate comparator decision errors, incomplete settling, and other error sources that may cause the residue voltage to exceed 0.5 LSB, 1-bit amplification redundancy is introduced between each stages. Finally, the architecture is chosen as 3+1-3+1-6 bits, corresponding to 4 bits for the first and second stages and 6 bits for the back-end stage.

The top-level diagram of the proposed pipeline loop-unrolled SAR ADC is shown in Figure 2.2. The proposed ADC adopts a three-stage architecture. Loop-unrolled SAR ADCs are used as sub-ADCs. The resolutions of the three stages are 4-bit, 4-bit, and 6-bit, respectively. 1-bit redundancy for each inter-stage. The waveform of the pipelined Lu-SAR ADC is shown as Figure 2.3.

For a pipelined SAR ADC, each stage should have enough time for sampling, CDAC settling, comparator decision, and residue amplification. The sampling frequency for this work is $300MHz$, so the period is approximately 3.3 ns. The time plan for this ADC is shown in Table 2.1

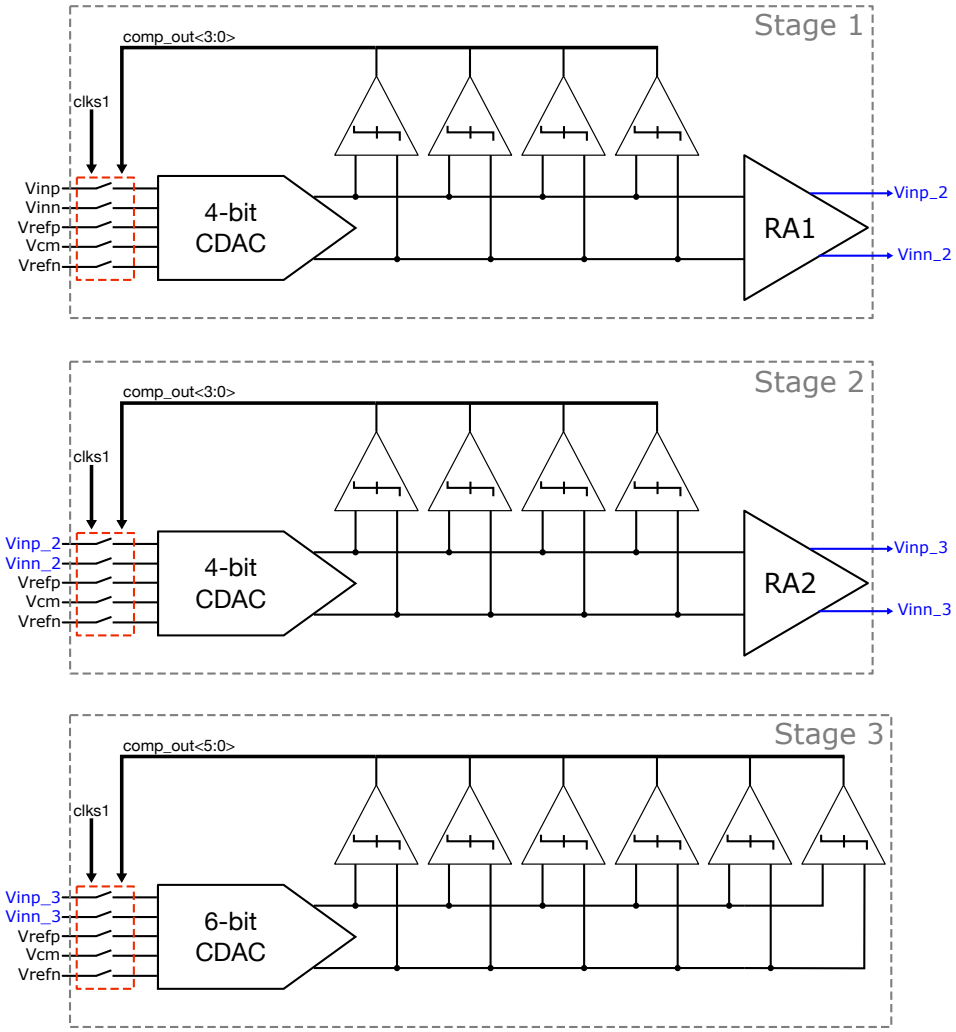


Figure 2.2: Top Level Schematic

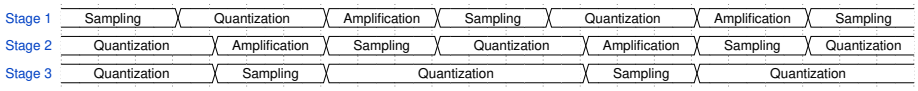


Figure 2.3: Waveform of pipelined Lu-SAR ADC

	Stage 1	Stage 2	Stage 3
Sampling	1ns	1ns	1ns
Quantization	1.3ns	1.3ns	2.3ns
Amplification	1ns	1ns	-

Table 2.1: Time Budget Summary for the Proposed ADC

2.4 Nonlinearity Sources

The main nonlinearity sources include the sampling nonlinearity in the first stage, comparator offsets in the sub-ADCs, capacitor mismatch in the CDACs, and the nonlinearity of the open-loop residue amplifiers. These nonlinearity sources are analyzed and modeled in this chapter.

2.4.1 Sampling nonlinearity

The sampling nonlinearity introduced by the switch has already been well studied in [1], so only the key points are summarized here for completeness. There are two main contributors to sampling distortion. The first is charge injection from the MOS switch. When the sampling switch turns off, part of its channel charge is transferred to the sampling capacitor, and because this charge depends on the input voltage, it introduces an input-dependent offset. Techniques such as bottom-plate sampling can reduce this effect by ensuring that the injected charge is largely independent of the signal. The second contributor is the input-dependent on-resistance of the sampling switch. Since the gate-source voltage of the MOS switch varies with the input signal, its on-resistance also changes, which makes the sampling time constant a function of the input voltage. This results in a nonlinear relationship between the actual sampled value and the input signal when the available sampling time is limited. A bootstrapped switch can keep the gate-source voltage nearly constant during sampling, making the switch resistance almost independent of the input and significantly reducing this form of nonlinearity. More detailed derivations and explanations of these effects can be found in [1].

2.4.2 Comparator offsets

The effect of comparator offsets in a standalone Lu-SAR ADC has already been analyzed in detail in our previously published work[9]. Here we only summarize the main conclusions for completeness. In a Lu-SAR architecture, each comparator only decides the thresholds belonging to one level of the binary search. As a result, the individual offsets from different comparators appear at different positions in the code domain, forming quasi-periodic deviations of the quantization thresholds. These deviations directly translate into a quasi-periodic INL pattern and generate spurs in the output spectrum. Behavioral simulations in the previous work show that, for a standalone Lu-SAR ADC, the standard deviation of comparator offsets should be kept below roughly 0.125 LSB; otherwise, both SFDR and SNDR degrade noticeably. These results serve as the basis for the offset requirement used in the system-level design of the pipelined Lu-SAR ADC in this thesis.

When a Lu-SAR ADC is put in a pipelined architecture with amplification redundancy between stages, the effect of comparator offsets can be greatly reduced. The pipeline ADC in this work consists of Stage 1 (4-bit Lu-SAR), Stage 2 (4-bit Lu-SAR), and Stage 3 (6-bit Lu-SAR). Two residue amplifiers are inserted between Stage 1 and Stage 2, and between Stage 2 and Stage 3, respectively.

With 1-bit amplification redundancy, the allowable residue range after each stage is extended from ± 0.5 LSB to ± 1 LSB, as discussed in section 2.3.3. This means that small decision errors caused by comparator offsets can be tolerated

by subsequent stages. When the comparator offsets are within 0.5 LSB, the ADC monotonicity is ensured, and the residue voltages will always remain within the ±1 LSB range. In contrast, the ADC monotonicity could be damaged if any comparator offset is larger than 0.5 LSB. Therefore, for the stages with inter-stage redundancy in a pipelined Lu-SAR ADC, comparator offsets smaller than 0.5 LSB can be covered by the redundancy and corrected by the quantization of the following stages.

The input differential range is ±0.8 V, so the LSB of Stage 1 and Stage 2 is $1.6/2^4 = 100$ mV. To guarantee proper operation, the comparator offsets in these stages should be smaller than 50 mV.

For the back-end stage, the linearity requirement is releaxed by the inter-stage gain, so the the requirement for comparator offsets is also releaxed.

To verify this analysis and find a maximum comparator offsets in design requirement, a system-level behavioral model of the proposed three-stage pipelined Lu-SAR ADC is built in MATLAB. The model is simulated under different levels of comparator offset deviation. Figure 2.4 shows the simulated SFDR versus the comparator offset deviation. Both the mean SFDR and the mean value of the lowest 10% of results are plotted. It can be seen that the overall SFDR degradation decreases more rapidly when the comparator offset deviation is around 20 mV. This is because when the comparators' offset is larger than 0.5 LSB, the redundancy cannot cover the error, which is consistent with the previous analytical result.

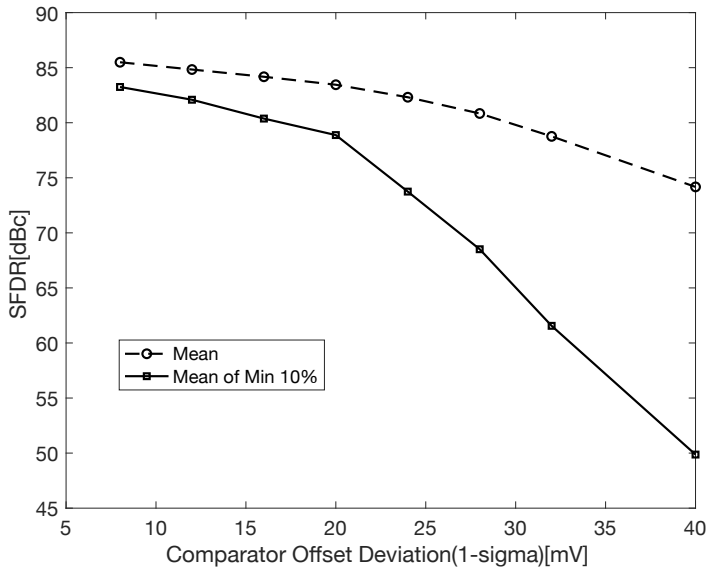


Figure 2.4: SFDR versus comparator offset deviation of the proposed pipelined ADC.

Therefore, comparator offsets in a pipelined Lu-SAR ADC may not require calibration if redundancy, inter-stage gains, and uncalibrated comparator offsets

are designed properly.

2.4.3 Capacitor Mismatch

The capacitor mismatch in the CDACs introduces INL and DNL errors in the sub-ADCs, which leads to distortion. According to [11], the INL caused by capacitor mismatch can be approximated as

$$INL \approx \frac{1}{\sqrt{4m}} \frac{\Delta C}{C_u} V_{\mathrm{REF}} \tag{2.10}$$

where m is the number of unit capacitors, ΔC is the standard deviation of the unit capacitors, C_u is the unit capacitance, and V_{REF} is the reference voltage. The INL is typically required to be smaller than 1 LSB, so that the requirement of the relative capacitor mismatch($\Delta C/C$) is

$$\frac{\Delta C}{C_u} < \sqrt{4m} \cdot \frac{V_{\mathrm{LSB}}}{V_{\mathrm{REF}}} \tag{2.11}$$

In the proposed 12-bit ADC, 1 LSB corresponds to $V_{\mathrm{REF}}/2^{12}$. Based on this, the capacitor deviation requirements for the three stages can be derived as follows. For the second stage, the effective LSB is amplified by the gain of the first stage, A_1. For the third stage, the effective LSB is amplified by the product of the gains of the first and second stages, $A_1 \times A_2$. Therefore, the allowable capacitor mismatch for each stage must be scaled accordingly to ensure that the INL remains below 1 LSB at the ADC output.

Specifically, the standard deviation of the unit capacitors in each stage should satisfy:

$$\begin{aligned}
\frac{\Delta C_{1,unit}}{C_{1,unit}} &< \frac{\sqrt{4m_1}}{2^{12}} = \frac{1}{2^9} = 1.95 \times 10^{-3} \\
\frac{\Delta C_{2,unit}}{C_{2,unit}} &< \frac{\sqrt{4m_2}}{2^{12}} \cdot A_1 = \frac{1}{2^6} = 1.57 \times 10^{-2} \\
\frac{\Delta C_{3,unit}}{C_{3,unit}} &< \frac{\sqrt{4m_3}}{2^{12}} \cdot A_1 \cdot A_2 = \frac{1}{2^{3.5}} = 8.8 \times 10^{-2}
\end{aligned} \tag{2.12}$$

The minimum MOM capacitor in the STM65 library is 3.63 fF, with a standard deviation of approximately 13 aF. The relative mismatch is therefore

$$\frac{13 \text{ aF}}{3.63 \text{ fF}} \approx 3.6 \times 10^{-3}$$

which is much smaller than the requirement for the second and third stage CDACs. Consequently, capacitor mismatch in these two stages is not expected to be a limiting factor.

A system-level model of the proposed pipelined Lu-SAR ADC including capacitor mismatch is built and simulated. In the simulation setup, the relative mismatch of the second and third stages is set to match that of the minimum unit capacitor, while the relative capacitor mismatch of the first stage is swept

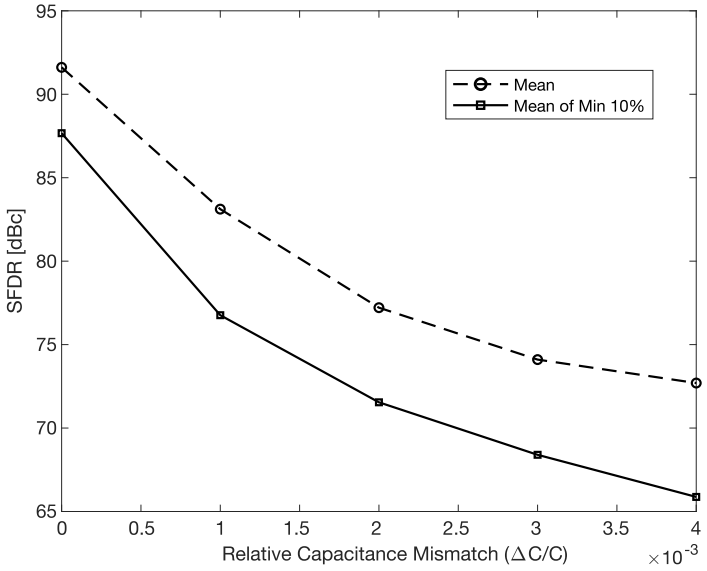


Figure 2.5: SFDR versus Relative Capacitor Mismatch of 1st stage

to observe its impact on SFDR. The resulting SFDR versus $\Delta C_1/C_1$ is shown in Figure 2.5.

For the first stage, a larger unit capacitor is used to meet the noise and matching requirements. The second stage also does not use the minimum capacitor to have a lower KT/C noise. Meanwhile, the capacitor value in each stage is also limited by the speed requirement, so the final values are chosen considering speed, matching, and noise. The capacitor values for the sub-CDACs are listed in Table 2.2.

	Stage 1	Stage 2	Stage 3
Unit [fF]	16.51	7.62	3.63
Std. Dev. [aF]	35	28	12
ΔC/C	2.12e-3	3.67e-3	3.31e-3
ΔC/C for INL $<$ 1 LSB	$<$ 1.95e-3	$<$ 15.6e-3	$<$ 88.4e-3
Total [fF]	264	120	116

Table 2.2: Capacitance values for CDACs.

Based on the analysis in Section 2.2, as long as the capacitor mismatch does not cause the residue voltage to exceed ± 1 LSB, the digital background calibration can recover the original data. Due to the requirement of conversion speed, the first-stage unit capacitor is chosen slightly smaller than the matching requirement in (2.12). Therefore, the capacitor mismatch in the first stage is still slightly worse than the requirement, and calibration is needed. The implementation of the

calibration will be discussed in a later section.

To verify that the residue voltage will not exceed ±1 LSB, the worst-case scenario of the first-stage CDAC is analyzed. In this CDAC, the MSB capacitor consists of 8 unit capacitors. The standard deviation of the MSB is

$$\sigma_{\mathrm{MSB}} = \sqrt{8} \times 35 \text{ aF} \approx 99 \text{ aF}.$$

The 3-sigma value is therefore approximately 300 aF. Assume that the MSB has the worst-case mismatch of +300 aF, and the remaining LSB capacitors have the opposite mismatch of −300 aF, which maximizes the residue voltage deviation. In this case, the maximum residue voltage deviation is

$$\Delta V_{\mathrm{residue}} = \frac{600 \text{ aF}}{16.51 \text{ fF}} \approx 0.036 \text{ LSB}.$$

This value is much smaller than ±1 LSB, which indicates that the residue voltage will remain within the recoverable range of the digital background calibration.

2.4.4 Residue amplifier nonlinearity

Power-efficient open-loop amplification in pipeline ADCs was first introduced in [12]. The motivation is to avoid the power and speed limitations of closed-loop designs. However, when the feedback is removed, the amplifier gain becomes much more sensitive to PVT variations, and the intrinsic device nonlinearity is also exposed. Therefore, both gain error and nonlinearity become important error sources. [13] The trans-conductance of a differential pair decreases as the input differential voltage increases. This leads to a smaller voltage gain at large input levels. As a result, the overall transfer curve of the amplifier becomes slightly compressed near the full-scale input, which causes harmonic distortion in the residue signal. The output residue voltage can be expressed as

$$V_{out,res} = A_1 V_{in,res} + A_2 V_{in,res}^2 + A_3 V_{in,res}^3 + \cdots , \tag{2.13}$$

where A_1 is the small-signal gain, and A_2, A_3, etc represent the nonlinear coefficients.

The impact of the gain error of the residue amplifier has already been discussed in [14]. Therefore, in this section, we only focus on analyzing the nonlinear part of the open-loop residue amplifier.

A behavior level model of amplifier nonlinearity in pipleline ADCs, as shown in Figure 2.6, is build. The transfer function of the model is

$$V_{out} = V_{in} + e_q + \frac{A(-e_q)}{A_0} \tag{2.14}$$

where e_q is quantization error; $A(\cdot)$ is the nonlinear transfer function of the amplifier; A_0 is the nominal gain. We can see that when the amplifier is ideal($A(-e_q) = A_0 \cdot e_q$), the V_{out} is simply equals to V_{in}. The model is linear. However, when the residue amplifier is nonlinear, its transfer curve is no longer a straight line. An example of nonlinear transfer curve, with third and fifth order harmonic included, is shown in Fig. 2.7. Based on this amplifier characteristic, the resulting nonlinear transfer curve of the overall ADC model is plotted in Fig. 2.8.

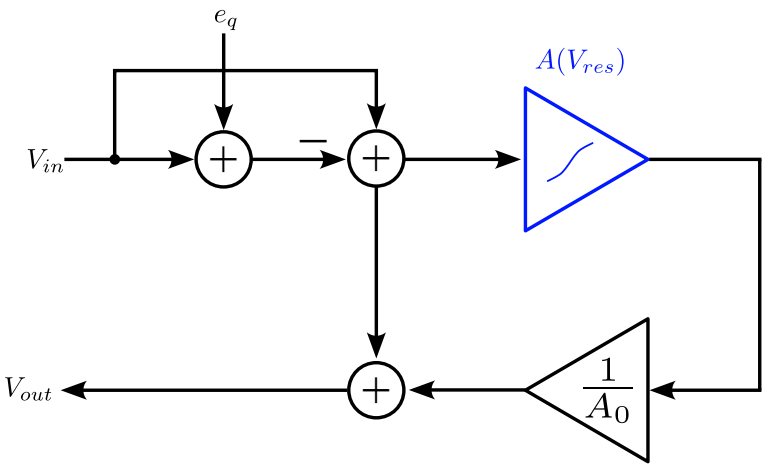


Figure 2.6: Block diagram of behavior model of amplifier nonlinearity in pipleline ADCs

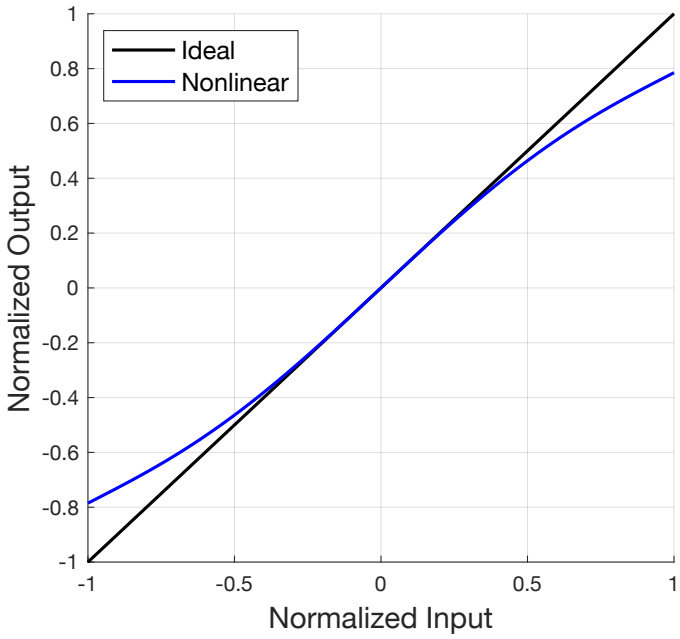


Figure 2.7: Transfer curve of residual amplifiers with nonlinearity

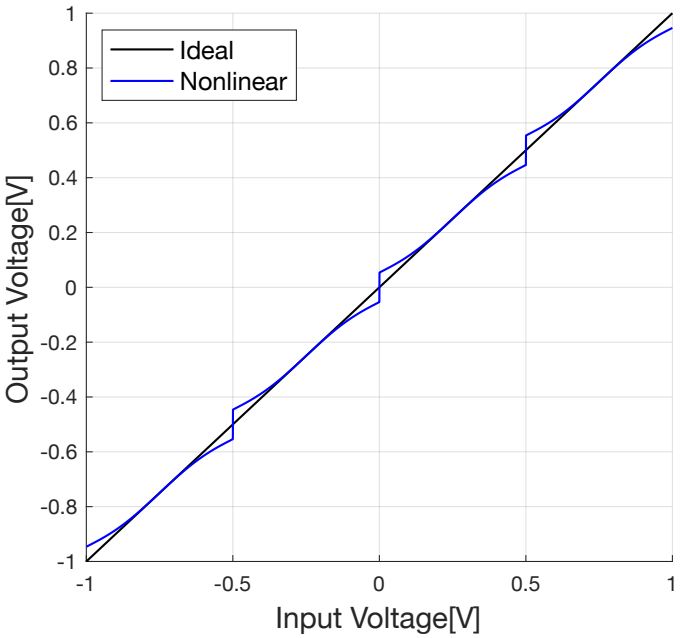


Figure 2.8: Transfer curve of behavior model with nonlinearity

In Chapter 4, a background calibration method based on the LMS algorithm is used to calibrate the nonlinearity of the open-loop residue amplifiers in real time. The basic idea is to model the inverse transfer curve of the residue amplifier as a polynomial function and implement this inverse in the digital domain. To verify this concept, an polynomial fit model is applied to the residue amplifier in the behavioral level, as shown in Figure 2.9 The poly-fitted inverse transfer curve of the amplifier is shown in Figure 2.10, and the transfer function of Figure 2.9 is:

$$V_{out} = V_{in} + e_q + A^{-1}_{poly-fit}(A(-e_q)) \approx V_{in} \tag{2.15}$$

So that the corrected overall transfer curve is shown in Figure 2.11.

To provide an initial guideline for designing the nonlinearity of the residue amplifier, a behavioral model of a 12-bit pipeline-SAR ADC is built. In this case, the amplifier is modeled with nonlinearity, while all other blocks remain ideal. The nonlinear parameters of the amplifier model are chosen such that, when the input sine-wave amplitude is 50 mV, the FFT of the amplifier output shows a THD of about –35 dB, with the third-order harmonic at –35 dB and the fifth-order harmonic at –60 dB. Under this condition, the output spectrum of the ADC is also shown, where a noticeable performance degradation appears due to the amplifier nonlinearity. Next, we apply a third-order polynomial fitting to the inverse transfer curve of the amplifier, including both the gain term and the third-order term. After the polynomial fitting, the FFT result shows that the third-order harmonic is greatly reduced, and the overall THD also improves.

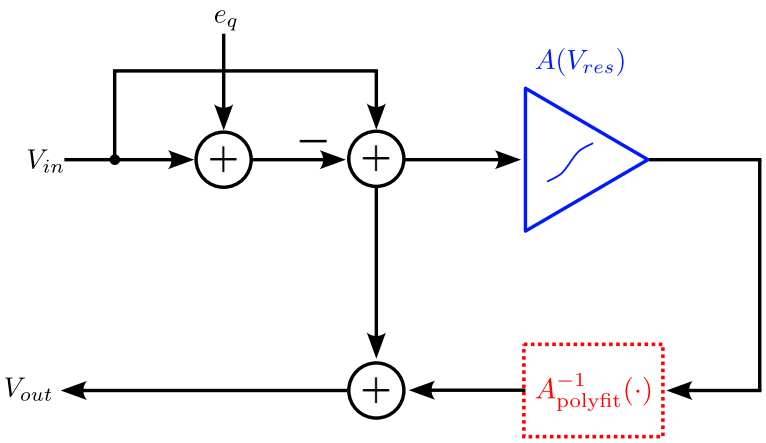


Figure 2.9: Block diagram of behavior model of amplifier nonlinearity in pipleline ADCs with inverse poly-fit

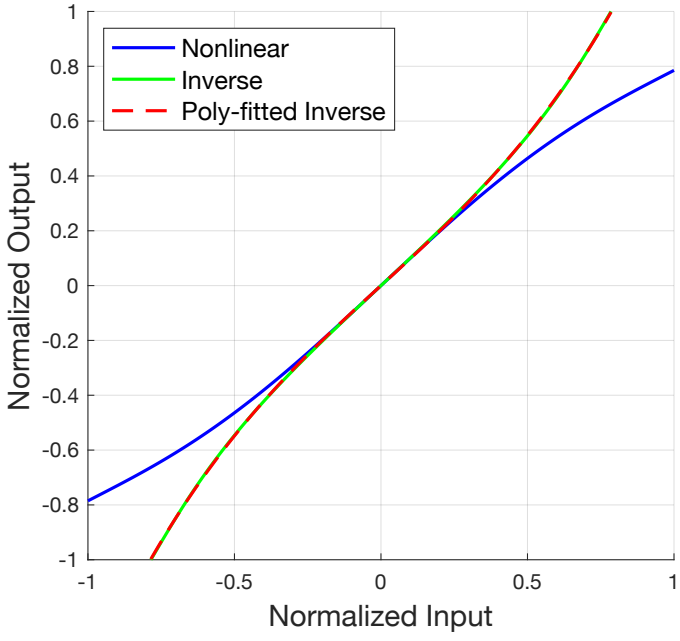


Figure 2.10: Transfer curve of residual amplifiers with nonlinearity

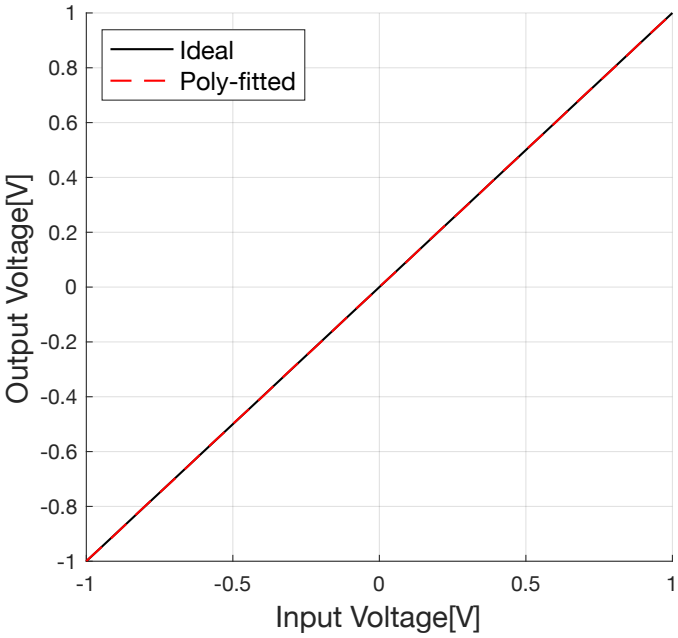


Figure 2.11: Transfer curve of behavior model with nonlinearity with poly-fit correction

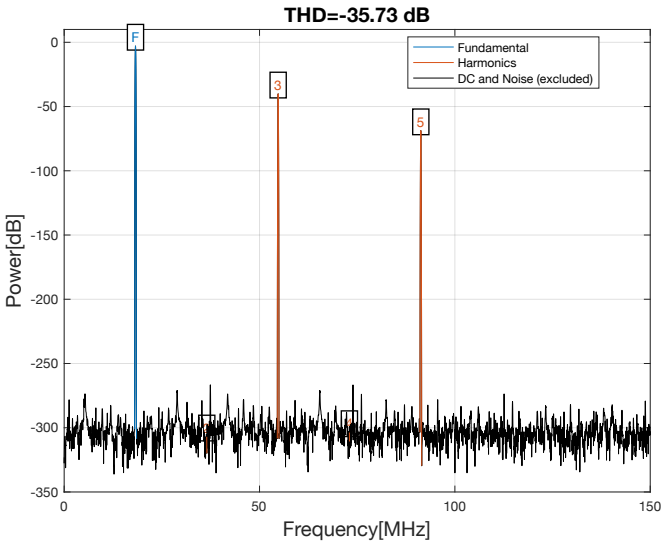


Figure 2.12: Spectrum of output of nonlinear amplifier(Behavior Level)

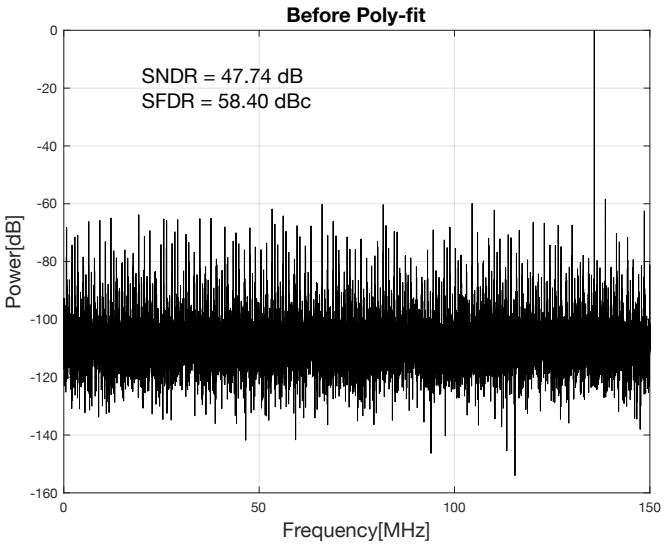


Figure 2.13: Spectrum of proposed ADC with nonlinear amp.(Behavior Level)

The corresponding ADC output spectrum also shows a significant improvement. These results indicate that an amplifier with THD better than –35 dB, third-order distortion below –35 dB, and fifth-order distortion below –60 dB can be effectively corrected by the proposed polynomial-fit based calibration method.

It can be seen that after the polynomial fitting, the transfer characteristic becomes very close to the ideal linear curve, which indicates that the polynomial model can effectively calibrate the amplifier nonlinearity.

2.5 Noise Analysis

In a pipeline ADC, the total input-referred noise can be represented by a superposition of quantization noise and the circuit noise of each stage, as shown by **??**

$$v_{in,tot}^2 = v_{q,n}^2 + v_{s1,n}^2 + \frac{v_{s2,n}^2}{A_1^2} + \frac{v_{s3,n}^2}{A_1^2 \cdot A_2^2} \tag{2.16}$$

where $v_{q,n}^2$ is the quantization noise power, $v_{s1,n}^2$, $v_{s2,n}^2$, and $v_{s3,n}^2$ are the noise powers of Stage 1, Stage 2, and Stage 3, respectively, and A_1 and A_2 are the gains of the first and second residue amplifiers. The noise from later stages is divided by the square of the preceding amplifier gains when referred to the ADC input.

The circuit noise of each stage and the quantization noise can be expressed as

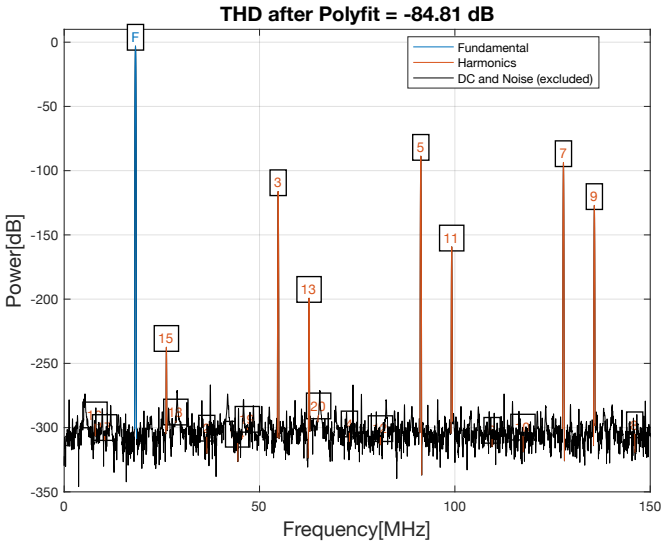


Figure 2.14: Spectrum of output of poly-fitted amplifier(Behavior Level)

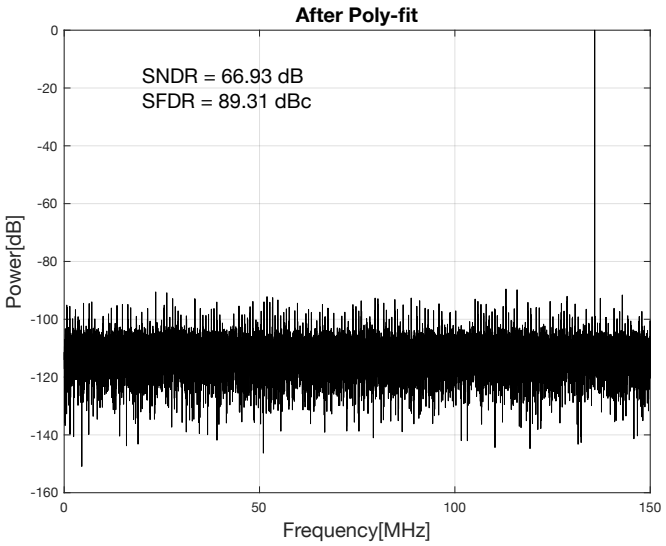


Figure 2.15: Spectrum of proposed ADC with poly-fitted amp.(Behavior Level)

$$\begin{aligned} v_{s1,n}^2 &= 2\frac{kT}{C_1} + v_{n,RA1}^2 \\ v_{s2,n}^2 &= 2\frac{kT}{C_2} + v_{n,RA2}^2 \\ v_{s3,n}^2 &= 2\frac{kT}{C_3} + v_{n,comp}^2 \\ v_{q,n}^2 &= \frac{(\mathrm{LSB})^2}{12} \end{aligned} \tag{2.17}$$

where C_1, C_2, and C_3 are the single-ended sampling capacitors of Stage 1, Stage 2, and Stage 3, respectively. $v_{n,RA1}^2$ and $v_{n,RA2}^2$ are the input-referred noise powers of the first and second residue amplifiers, and $v_{n,comp}^2$ is the input-referred noise power of the comparator in the last stage. Since the circuit adopts a fully differential structure, the thermal noise from sampling capacitors is doubled, so the total kT/C noise term becomes $2kT/C$.

Because of the amplification redundancy between stages, the comparator noise in the first and second stages does not affect the final digital output. In this case, the overall input-referred noise of the pipeline ADC is mainly contributed by the quantization noise, the kT/C noise from the first stage, and the noise of the first residue amplifier. The inter-stage gain suppresses the noise from later stages.

Based on the noise model discussed above, the noise budget of the proposed pipe-Lu-SAR ADC is analyzed. The SNDR requirement is larger than 60 dB, and the differential input peak-to-peak voltage is 1.6 V. The corresponding LSB is

$$\mathrm{LSB} = \frac{V_{pp}}{2^{12}} = \frac{1.6}{4096} = 0.3906 \text{ mV}.$$

The quantization noise power is

$$v_{qn}^2 = \frac{\mathrm{LSB}^2}{12} = 1.27 \times 10^{-8} \text{ V}^2.$$

The first-stage total sampling capacitor C_1 is selected as 264 fF. For a fully differential structure, the sampling thermal noise is

$$v_{s1}^2 = 2\frac{kT}{C_1} = 3.14 \times 10^{-8} \text{ V}^2,$$

which is about 4.3 times larger than the quantization noise.

Assuming the full-scale differential input is a sine wave, the signal power is

$$P_{\text{signal}} = \left(\frac{V_{pp}/2}{\sqrt{2}}\right)^2 = 0.32 \text{ V}^2.$$

By considering only the quantization noise and the first-stage kT/C noise, the noise-limited SNDR can be estimated as

$$\mathrm{SNDR} = 10\log_{10}\left(\frac{P_{\text{signal}}}{v_{qn}^2 + v_{s1}^2}\right) = 66.7 \text{ dB},$$

If the target SNDR is 60 dB, the total allowed input-referred noise power is

$$v^2_{\text{noise,allowed}} = \frac{P_{\text{signal}}}{10^{\text{SNDR}_{\text{target}}/10}} = 3.2 \times 10^{-7}\ \text{V}^2.$$

After subtracting the quantization noise and the first-stage sampling noise, the remaining noise budget for the first residue amplifier is

$$v^2_{n,other,\max} = v^2_{\text{noise,allowed}} - (v^2_{qn} + v^2_{s1}) = 2.52 \times 10^{-7}\ \text{V}^2.$$

The input-referred noise power budget for other noise sources, mainly the first stage residue amplifier, are about 19.8 times of the quantization noise to meet the requirement of 60 dB SNDR.

Chapter 3
Design

3.1 Residual Amplifier

The first residual amplifier (RA) is implemented as a two-stage open-loop structure, as shown in Figure 3.1.

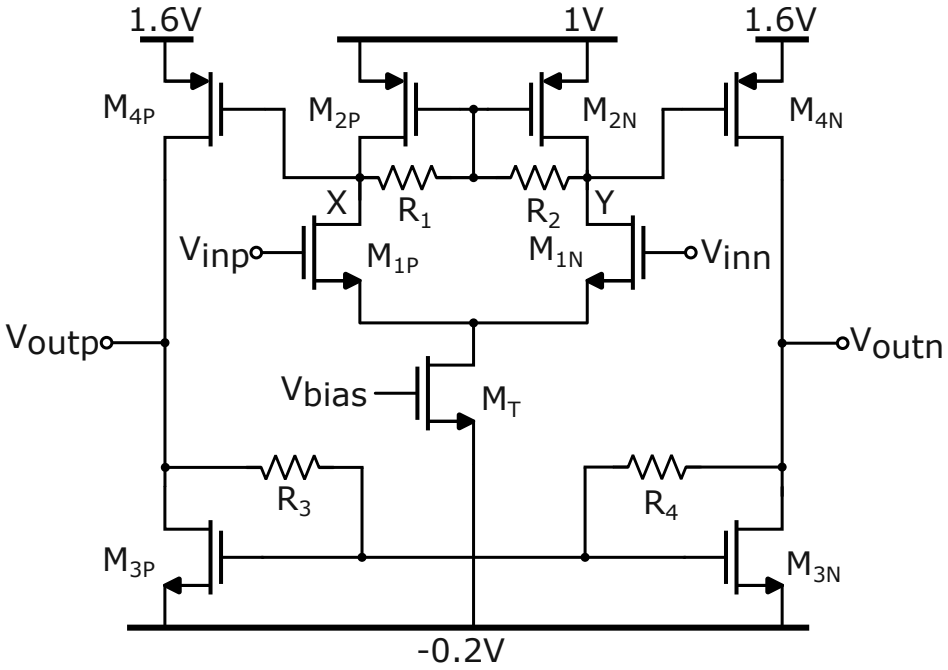


Figure 3.1: Schematic of 1st Residual Amplifier

The first stage is a differential pair with a current-source load. The second stage is a common-source amplifier with a current-source load, which further amplifies the signal to achieve the required inter-stage gain. In addition, To ensure the output signal swing, the second-stage amplifier has upper and lower rails of 1.6 V and -0.2 V, respectively. Therefore, high-voltage MOS transistors capable of operating under a 1.8 V supply are employed in this stage.

Both stages employ simple resistive common-mode feedback (CMFB) networks. The resistive CMFB is chosen mainly for simplicity and high-speed performance. Unlike active CMFB circuits that require auxiliary amplifiers and may introduce additional poles or settling delay, the resistive CMFB provides a purely resistive feedback path with no extra dynamic components, resulting in faster settling and improved stability, which is an important advantage for high-speed open-loop amplifiers.

The second RA adopts a simplified structure that only includes the first stage of the two-stage amplifier.

The performance of the proposed RAs is shown in Table 3.1 and 3.2.

	TT	SS	FF
Output Load[fF]	120		
Gain	8.31	8.77	7.70
-3 dB BW[GHz]	1.42	1.27	1.59
Input-referred Noise[mV]	0.180	0.184	0.181
Power[mW]	7.3		

Table 3.1: Performance Summary of the 1st RA

	TT	SS	FF
Output Load[fF]	116		
Gain	4.21	4.53	3.85
-3 dB BW[GHz]	1.06	0.89	1.25
Input-referred Noise[mV]	0.156	0.141	0.157
Power[mW]	1.7		

Table 3.2: Performance Summary of the 2nd RA

Since their design principles are similar, only the design consideration of the first RA is discussed in detail in this section.

3.1.1 Common-Mode Voltage

The amplifier and comparators in the following stage require the output common-mode voltage of this amplifier to be 600 mV. This design does not employ an active CMFB with a reference common-mode voltage. Therefore, the 600 mV common-mode voltage is achieved by appropriately tuning the transistor sizes. In the output stage, the current of transistor M_3 is given by

$$I_{\mathrm{D3}} = \frac{1}{2}\mu_n C_{\mathrm{ox}}(\frac{W}{L})_n(V_{\mathrm{out,CM}} - V_{\mathrm{TH,N}})^2(1 + \lambda V_{\mathrm{out,CM}}) \tag{3.1}$$

The current of M_4 is shown as 3.2

$$I_{\mathrm{D4}} = \frac{1}{2}\mu_p C_{\mathrm{ox}}(\frac{W}{L})_p(V_{\mathrm{XY,CM}} - V_{\mathrm{DD}} - V_{\mathrm{TH,P}})^2(1 + \lambda(V_{\mathrm{DD}} - V_{\mathrm{out,CM}})) \tag{3.2}$$

They should satisfy $I_{\mathrm{D3}} = I_{\mathrm{D4}}$. If we ignore the channel length modulation, we can have 3.3

$$V_{\mathrm{out,CM}} = \sqrt{\frac{\mu_p(W/L)_3}{\mu_n(W/L)_4}}(V_{\mathrm{XY,CM}} - V_{\mathrm{DD}} - V_{\mathrm{TH,P}}) + V_{\mathrm{TH,N}} \tag{3.3}$$

Here, $V_{\mathrm{XY,CM}}, V_{\mathrm{out,CM}}$ is the common mode output voltage of the first and second stages, respectively. Similarly, we can have 3.4

$$V_{\mathrm{XY,CM}} = \sqrt{\frac{\mu_n(W/L)_1}{\mu_p(W/L)_2}}(V_{\mathrm{in,CM}} - V_{\mathrm{DD}} - V_{\mathrm{TH,P}}) + V_{\mathrm{TH,N}} \tag{3.4}$$

Equations 3.3 and 3.4 gives an initial estimation of the size ratio to achieve the target common-mode level. However, due to second-order effects such as channel length modulation, the actual common-mode voltage could be different with the calculated value, so the ratio still needs to be fine-tuned through simulation.

When there is a mismatch between the NMOS and PMOS devices, the channel length modulation will also influence the common-mode balance. For example, if the NMOS device is slightly smaller, its current tends to be smaller, and the circuit must increase the output common-mode voltage to raise $V_{DS,n}$ to achieve enough current. When channel length modulation is considered, the increase in $V_{DS,n}$ also increases the NMOS current, while the corresponding decrease in $V_{SD,p}$ reduces the PMOS current. As a result, the required change in common-mode voltage is smaller than the situation without considering channel length modulation. Therefore, channel length modulation helps the common-mode balance slightly.

3.1.2 Differential Input Linear Range

Unlike closed-loop amplifiers, where the feedback keeps the input differential voltage close to zero, the input of an open-loop amplifier directly follows the signal itself. As a result, the input range is determined by the transistor operation regions. The transistors should remain in saturation without cutoff or entering the triode region across the input range.

The input voltage should keep M_{1P} and M_{1N} on, and keep M_T saturated, so we have:

$$V_{\mathrm{in}} > V_{\mathrm{TH,N}} + V_{\mathrm{OV,T}} \approx V_{\mathrm{GS,T}} \tag{3.5}$$

where $V_{OV,T}$ and $V_{\mathrm{GS,T}}$ are the overdrive and gate-source voltage of the tail transistor. From the output side, the output node voltage must keep both the input transistors and the load transistors in saturation, as shown in Figure 3.2.

The saturation requirements of the NMOS input pair and the PMOS load devices impose the following constraints:

$$\begin{aligned} V_{\mathrm{in}} - V_{\mathrm{X,Y}} &< V_{\mathrm{TH,N}} \\ V_{\mathrm{X,Y}} &< V_{\mathrm{XY,CM}} + V_{\mathrm{TH,P}} \end{aligned} \tag{3.6}$$

Here, $V_{\mathrm{XY,CM}}$ is the common mode level of nodes X and Y.

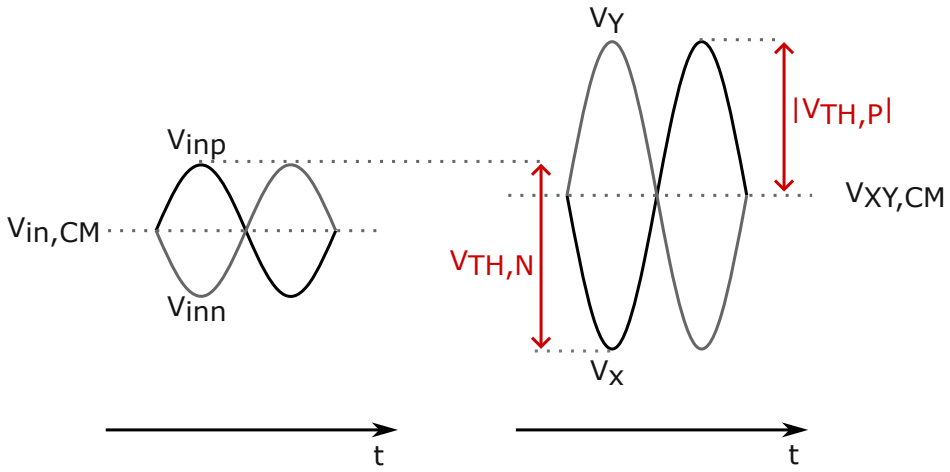


Figure 3.2: Maximum linear range of the proposed amplifier

The input and internal node voltages can be expressed using their common mode and differential components:

$$\begin{aligned} V_{\text{in}} &= V_{\text{in,CM}} + \frac{V_{\text{in,diff}}}{2} \\ V_{\text{X,Y}} &= V_{\text{XY,CM}} + \frac{V_{\text{XY,diff}}}{2} \\ V_{\text{XY,diff}} &= -A_{\text{1st}} \cdot V_{\text{in,diff}} \end{aligned} \tag{3.7}$$

Here, A_{1st} is the gain of the first stage.

Substituting the relations in (3.7) into the saturation limits in (3.5) and (3.6), we obtain three constraints on the maximum allowable differential input swing:

$$\begin{aligned} V_{\text{in,diff}} &< V_{\text{in,CM}} - V_{GS,T} \\ V_{\text{in,diff}} &< \frac{(V_{\text{XY,CM}} - V_{\text{in,CM}}) + V_{\text{TH,N}}}{1 + A_{\text{1st}}} \\ V_{\text{in,diff}} &< \frac{V_{\text{TH,P}}}{A_{\text{1st}}} \end{aligned} \tag{3.8}$$

The allowable differential input swing is determined by the smaller of these constraints. This result shows that both internal common mode levels and device threshold voltages directly determine the linear operating range. A larger first-stage gain also reduces the maximum linear input swing, so the gain selection must trade off with the common mode selection and input linear swing.

3.2 Loop-Unrolled SAR ADC

This design consists of three Lu-SAR ADC stages: two 4-bit stages and one 6-bit back-end stage. A top-level schematic of the Lu-SAR ADC is shown in

Figure 2.1. Since the three sub-ADCs share the same architecture and circuit topology, only the 6-bit back-end stage is described in detail here. It mainly includes bootstrapped sampling switches, a 6-bit CDAC, six comparators, and six dynamic delay cells.

3.2.1 Double-Tail Comparator

The schematic of the proposed double-tail comparator is shown in Figure 3.3. The fully dynamic double-tail comparator has two phases: the pre-charge phase and the comparison phase. During the pre-charge phase, the clock signal is low. The tail transistors M_{T1} and M_{T2} are turned off. The pre-charge switches M_{2P} and M_{2N} are turned on. The output nodes of the first stage are pre-charged to V_{DD} through M_{2P} and M_{2N}. The output nodes V_{outp} and V_{outn} are discharged to ground.

When the clock goes high, the comparator enters the comparison phase. The tail transistors are turned on, and the differential input pair M_{21} and M_{1N} start to pre-amplify the input voltage. The voltage difference between the output of the first stage differential pair is fed to the second stage. The side with the higher input voltage will have a larger voltage drop on the input of the second stage, which results in amplified different discharge at the output nodes. The cross-coupled inverters form a positive feedback loop on output nodes, which quickly amplifies the small voltage difference until one output is pulled up to V_{DD} and the other remains at ground.[15]

The double-tail structure has individual stages for pre-amplification and latch, which reduces the DC offset, input-referred noise, and kick-back noise. Compared to the conventional strong-arm comparator, the number of stacked transistors in each stage is less, so it can work under a lower supply voltage. Moreover, the fully dynamic operation doesn't consume static power.[16]

The input-referred noise, time constant, clock-to-output delay, and power consumption of the comparator are simulated. The transistor-level simulation results are shown in the Table 3.3.

Input-referred Offset	16 mV
Input-referred Noise	1.3 mV
Delay(clk-to-output)	120 ps

Table 3.3: Performance Summary of the Double-Tail Comparator

3.2.2 Bootstrapped Switch

The analysis and design process of the bootstrapped switch follows [17, 18]. The schematic of the proposed bootstrapped switch is shown in Figure 3.4. The bootstrapped switch operates in two phases: the reset (hold) phase and the sampling phase. During the reset (hold) phase, the clock signal is high. Transistors M_1 and M_2 are turned on, charging the top plate of the bootstrapped capacitor to V_{DD} and discharging the bottom plate to ground. At the same time, M6 is turned on

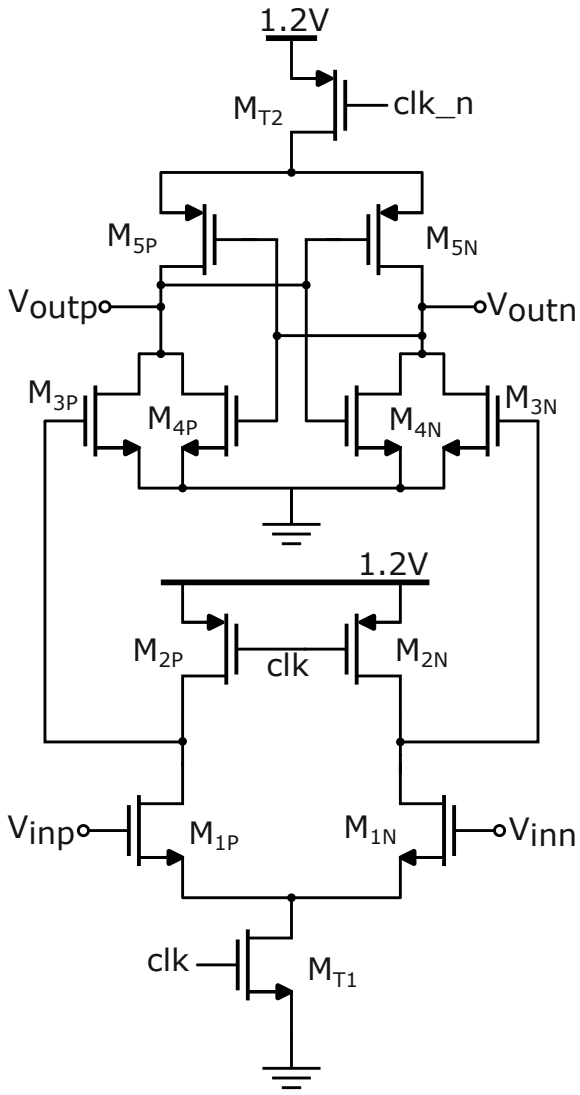


Figure 3.3: Schematic of Proposed Double-Tail Comparator

to pull node X to ground, which turns off the sampling switch M_s. The capacitor is thus pre-charged for the next sampling phase. M_5 is used to release the device stress of M_6 during this phase to improve its reliability.

When the clock signal goes low, the circuit enters the sampling phase. Transistor Ma turns on and enables M_4. With M_4 turned on, the top plate of the bootstrapped capacitor is connected to node X. This action turns on M_3 and M_s. As a result, the gate and source of M_s are connected to the top and bottom plates of the bootstrapped capacitor, respectively, forming a bootstrapped configuration. In this state, the gate-source voltage of Ms is approximately equal to V_{DD}, independent of the input signal voltage. Therefore, the on-resistance of M_s remains nearly constant over the full input range, which improves sampling linearity.

In addition, M_a and M_b are used to bootstrap the gate voltage of M_4, ensuring full switching of M_4 in both phases. Transistor M_c is used to provide a low resistance path in series with the gate of M_4, which helps the gate voltage of M_4 follow the bootstrap voltage more accurately and reduces delay during the switching transition. [11]

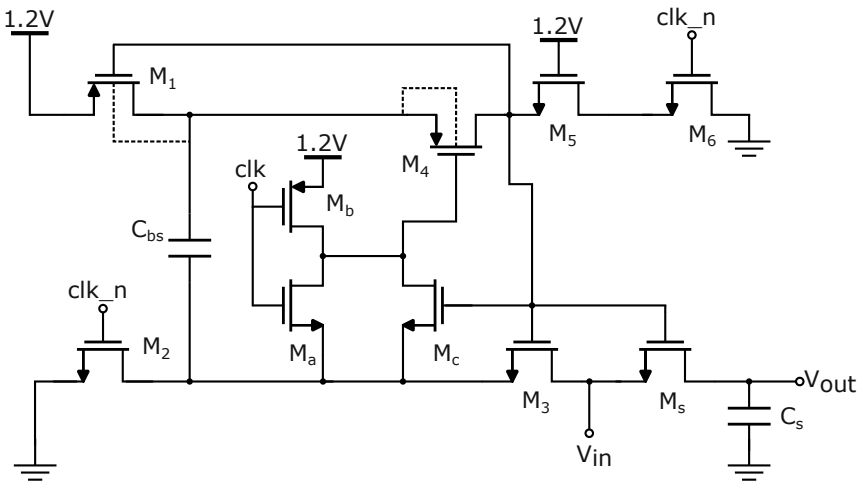


Figure 3.4: Schematic of Proposed Bootstrapped Switch

3.2.3 Delay Cell

Each delay cell is implemented using a ratioed NAND gate followed by a static logic buffer, as shown in Figure 3.5. Unlike normal ratioed logic, the pull-down transistor M_{PD} provides a strong discharge path when the clock (clk) is high. This pre-discharges the output node to low during the sampling phase. The delay cell output is used as the clock signal for the comparator, while the input clock of the delay cells is the sampling clock. In this way, all comparators are reset during sampling.

After sampling, M_{PD} is turned off. At this moment, both input nodes A and B are high because the previous comparator is still reset. When one of them goes low, meaning the previous comparator has finished the comparison, M_1 or M_2 turns

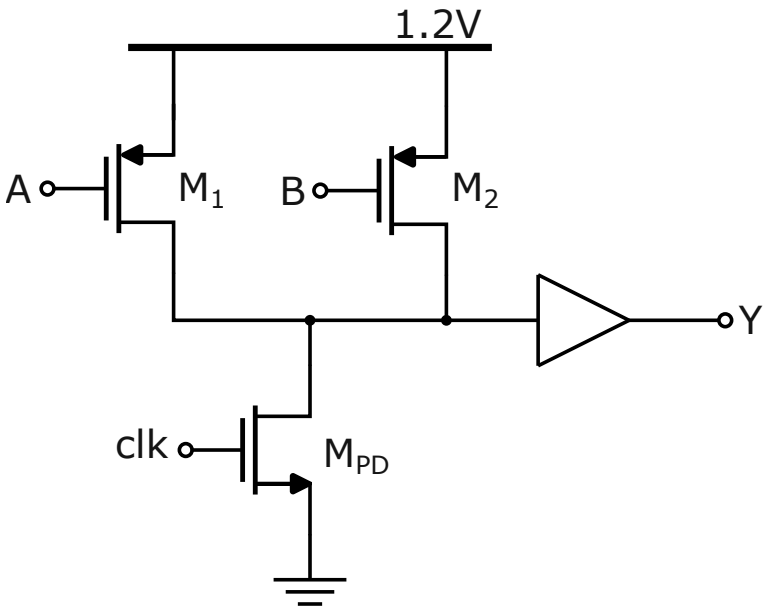


Figure 3.5: Schematic of the delay cells

on and charges the input node of the buffer. After a certain delay determined by the sizes of M_1, M_2, and the buffer, the output Y becomes high and then triggers the next comparator.

Each delay cell is placed right after the comparator to generate the enable signal for the next bit comparison. Different delay times are designed for different bits to achieve a balance between precision and speed: the MSB delay is longer to allow enough CDAC settling time, while the delay decreases for smaller bits to increase conversion speed.

Chapter 4
Calibration

4.1 Fundamental of Least-Mean-Sqaure Algorithm

The LMS algorithm has been widely applied to background calibration in both pipelined and SAR ADCs [13, 19]. A simplified block diagram of the LMS-based calibration system is shown in Figure 4.1. This algorithm follows the principle of adaptive equalization, which is one of the typical applications of the LMS method. More background information about the LMS algorithm and its application can be found in [20]. In this scheme, the analog input signal V_{in} is converted by the main ADC, whose transfer function deviates from the ideal due to gain error, nonlinearity, or bit-weight deviation. The original output of the under-calibrated ADC is then given to a tunable digital filter G. Its coefficients are continuously updated by the LMS loop. The output of $G(s)$ is the final corrected quantization result D_{out}, which also represents the estimated value of the original input $\hat{V}_{in}$.

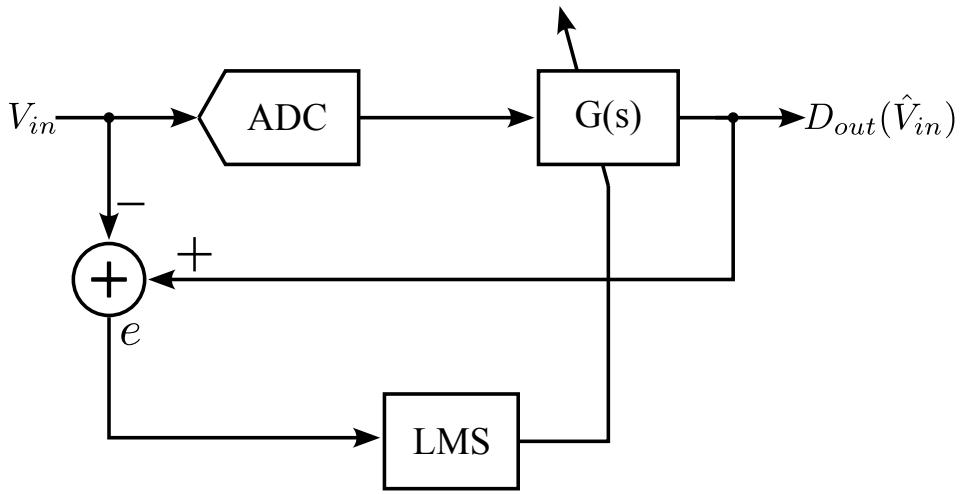


Figure 4.1: Simplified ADC Calibration Diagram based on LMS

The difference between the estimated output and the actual input forms the error signal:

$$e[n] = D_{out}[n] - V_{in}[n] \tag{4.1}$$

This error is used to evaluate the cost function:

$$J = E(e[n]^2) \tag{4.2}$$

which has a minimum value when the estimated output matches the input. By applying LMS principle, the coefficients inside $G(s)$ are adaptively updated to minimize J:

$$g_i[n+1] = g_i[n] + \mu e[n] \frac{\partial e}{\partial g_i} \tag{4.3}$$

where μ is the step size that controls convergence speed and stability. As the LMS loop iterates, G gradually converges to the inverse transfer function of the under-calibrated ADC, so that the transfer function from V_{in} to D_{out} is linear. Since the LMS loop operates continuously in the background, it does not interrupt the normal ADC conversion process. This makes it well-suited for compensating circuit parameters that vary slowly with temperature, voltage, or process. In this work, the parameters to be adaptively estimated are bit-weight deviation of sub-ADCs, the gain, and the nonlinearity of the residue amplifier.

4.2 Gain Calibration

Figure 4.2 shows the equalization-based gain calibration for the i-th stage in an M-stage pipeline ADC. The input to this stage is the residue from the previous stage, denoted R_{i-1}, and the stage produces a local quantization result D_i. The

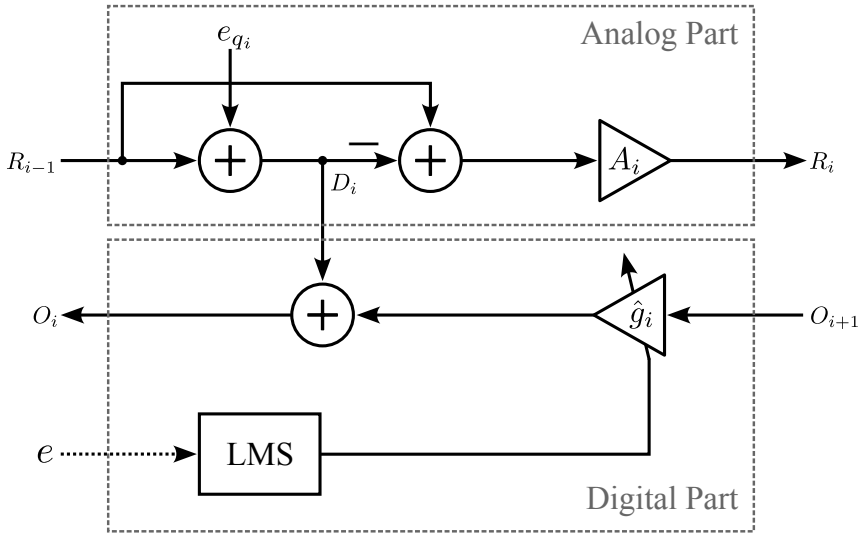


Figure 4.2: Block Diagram of $i-th$ Stge Gain Calibration

analog residue amplifier applies gain A_i to the remaining voltage, so the residue

delivered to the next stage is

$$R_i = A_i(R_{i-1} - D_i) \tag{4.4}$$

The following stages quantize R_i and produce a quantization output, denoted O_{i+1}. In the digital calibration path, O_{i+1} is timed by an estimated inverse gain $\hat{g}_i$ and added to D_i to recover the input of stage i:

$$O_i = D_i + \hat{g}_i\, O_{i+1} \tag{4.5}$$

and considering that for the last stage M, $O_M = D_M$, the recursion can be expanded as:

$$O_i = \sum_{k=i}^{M} \left(\prod_{j=i}^{k-1} \hat{g}_j \right) D_k \tag{4.6}$$

where the empty product, such as $\prod_{j=i}^{i-1}(\cdot)$, is defined to be 1. This definition is also suitable for other equations in this Chapter.

The final ADC output is then shown in 4.7

$$D_{out} = O_1 = \sum_{k=1}^{M} \left(\prod_{j=1}^{k-1} \hat{g}_j \right) D_k \tag{4.7}$$

The calibration goal is: make $\hat{g}_i$ approach $1/A_i$, so that the D_{out} matches the quantization value corresponding to the analog input. The error is defined that measures this mismatch at system level:

$$e[n] = D_{out}[n] - V_{in}[n] \tag{4.8}$$

According to the LMS principle, the update function can be defined as

$$\begin{aligned} \hat{g}_i[n+1] &= \hat{g}_i[n] + \mu e[n] \frac{\partial e}{\partial \hat{g}_i} \\ &= \hat{g}_i[n] + \mu e[n] \frac{\partial O_1}{\partial g_i} \\ &= \hat{g}_i[n] + \mu e[n] \left(\prod_{j=1}^{i-1} \frac{\partial O_j}{\partial O_{j+1}} \right) \frac{\partial O_i}{\partial \hat{g}_i} \\ &= \hat{g}_i[n] + \mu e[n] \left(\prod_{j=1}^{i-1} g_j[n] \right) O_{i+1} \end{aligned} \tag{4.9}$$

4.3 Nonlinearity Calibration

The idea of nonlinear background calibration is similar to the gain calibration. In gain calibration, a single coefficient $\hat{g}_i$, is used to estimate the inverse transfer curve of the residual amplifier. This method works well when the residue amplifier is linear enough, e.g. close-loop amplifier whose nonlinearity suppressed by feedback.

However, when an open-loop amplifier is used, its effective gain depends strongly on the input amplitude as mentioned in Section 2.4. A single gain coefficient is not enough to describe the amplifers' characteristic. The calibration must compensate for the input-dependent nonlinearity. To solve this problem, we need to model and fit the inverse transfer function of the open-loop amplifier in the digital domain.

Several modeling methods have been reported in previous works[To Be Cited], including piecewise and polynomial approximations. The piecewise model has a smaller computation cost, but its cost function is non-differentiable at the boundary points. In practice, this requires separate adaptation for each segment, and the global convergence of the algorithm becomes difficult to prove.

The polynomial model is a continuous and differentiable estimation of the amplifier characteristic, which satisfies the mathematical condition required by the LMS algorithm. Although it introduces more computation and requires multipliers in hardware implementation, it provides a unified formulation and ensures stable convergence in background calibration.

Therefore, a polynomial model including the first and third-order terms is adopted in this work to approximate the inverse nonlinear transfer function of the open-loop residue amplifier. The block diagram is shown in Figure 4.3. This nonlinearity calibration has the same LMS-based framework as the gain calibration described in the previous section, but with an extended third-order calibration path to fit the nonlinearity.

As shown in the Figure 4.3, the output of the following stages, O_{i+1}, is first processed by both a linear gain coefficient g_i and a third-order coefficient h_i. The corrected output of $i-th$ stage is:

$$O_i = D_i + \hat{g}_i\, O_{i+1} + \hat{h}_i\, O_{i+1}^3. \tag{4.10}$$

Similar to gain calibration, the update functions of the proposed nonlinearity calibration is shown as 4.11.

$$\begin{aligned}
\hat{g_i}[n+1] &= \hat{g}_i[n] + \mu e[n](\prod_{j=1}^{i-1} \frac{\partial O_j}{\partial O_{j+1}})\frac{\partial O_i}{\partial \hat{g}_i} \\
&= \hat{g}_i[n] + \mu e[n](\prod_{j=1}^{i-1} g_j[n] + 3\hat{h}_j[n]O_{j+1}^2)O_{i+1} \\
\hat{h_i}[n+1] &= \hat{h}_i[n] + \mu e[n](\prod_{j=1}^{i-1} \frac{\partial O_j}{\partial O_{j+1}})\frac{\partial O_i}{\partial \hat{h}_i} \\
&= \hat{h}_i[n] + \mu e[n](\prod_{j=1}^{i-1} g_j[n] + 3\hat{h}_j[n]O_{j+1}^2)O_{i+1}^3
\end{aligned} \tag{4.11}$$

4.4 Bit-weight Calibration

The capacitor mismatch causes bit weight deviation and leads to distortion [21]. The block diagram of the proposed LMS-based calibration scheme is shown in Figure 4.4.

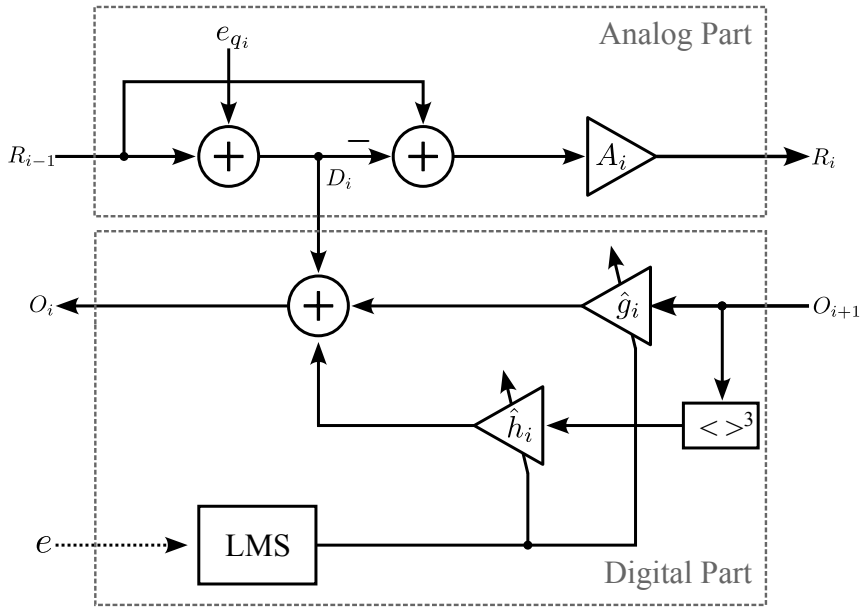


Figure 4.3: Block Diagram of $i-th$ Stage Nonlinearity Calibration

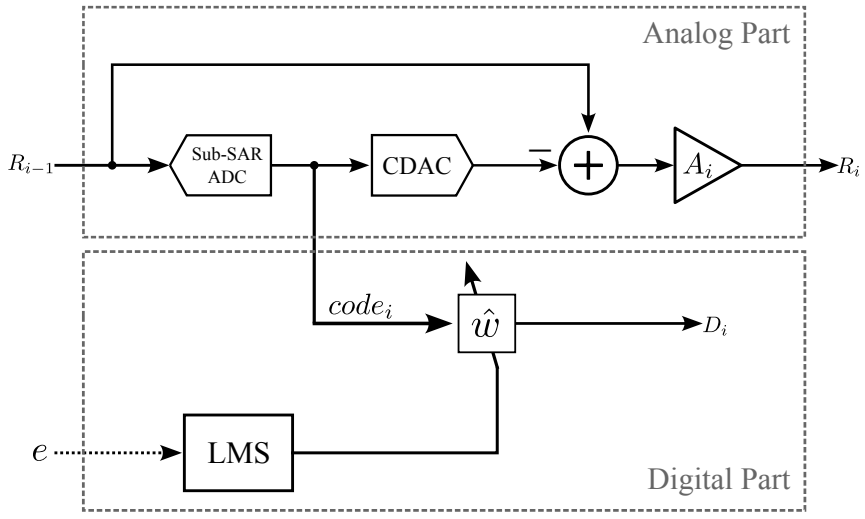


Figure 4.4: Block Diagram of $i-th$ Stage Bit-weight Calibration

The input voltage R_i is converted by the sub-SAR ADC and generates a N-bit digital code $code[N-1:0]$. The N-bit digital output is processed by a tunable digital filter that performs a weighted summation using adjustable digital weights $w[N-1:0]$. The local quantized result is

$$D_i = \sum_{j=0}^{N-1} code[j] \times w[j] \tag{4.12}$$

We apply the global error for bit-weight update as well:

$$e = D_{out} - V_{in} \tag{4.13}$$

As described in Section 2.4.1, only the capacitor mismatch of the first stage sub-ADC needs to be calibrated. The update equation of the first stage bit weights w is:

$$\begin{aligned}
\hat{w}_i[3:0][n+1] &= \hat{w}_i[3:0][n] + \mu e[n] \frac{\partial e}{\partial \hat{w}_i[3:0]} \\
&= \hat{w}_i[3:0][n] + \mu e[n] (\prod_{j=1}^{i-1} \frac{\partial O_j}{\partial O_{j+1}}) \frac{\partial D_1}{\partial \hat{w}_i[3:0]} \\
&= \hat{w}_i[3:0][n] + \mu e[n] (\prod_{j=1}^{i-1} g_j[n] + 3\hat{h}_j[n] O_{j+1}^2) \cdot code[3:0][n]
\end{aligned} \tag{4.14}$$

4.5 Foreground Calibration for Comparator Offsets

As discussed in Section 2.4, comparator offsets can degrade the linearity when a Lu-SAR ADC operates individually. However, in the proposed pipelined structure, such errors can be tolerated by inter-stage redundancy and further suppressed by the inter-stage gain. In this work, a low-cost foreground calibration scheme for standalone Lu-SAR ADCs is also proposed. Although this calibration is not implemented in the final pipelined ADC, it effectively improves the linearity of individual Lu-SAR converters. The detailed design and results of this calibration is in [9]. A brief summary is presented here for completeness.

The proposed calibration uses a single shared calibration CDAC (C-CDAC) to measure and store the offsets of all comparators during a foreground calibration phase. The stored digital codes are then used to compensate the comparator offsets during normal conversion. This method avoids the static power consumption of RDAC-based schemes and the PVT sensitivity of MOS-varactor-based calibration. A 6-bit 400 MS/s Lu-SAR ADC was implemented in 65 nm CMOS, and the simulation shows about 5–7 dB SFDR improvement after calibration. This approach provides a simple and low-cost solution for comparator offset calibration in high-speed Lu-SAR ADCs.

4.6 Modeling and Implementation

The proposed three-stage pipelined Lu-SAR ADC is modeled in MATLAB, including the major nonidealities such as first-stage capacitor mismatch, amplifier gain error, and nonlinearity. In the model, each residue amplifier has a nominal gain of 7.8, and a third-order nonlinear term is added to represent its distortion. The capacitor mismatch follows the data shown in Section 2.4, while all other circuit blocks are assumed to be ideal. To reduce computing complexity, the sign-sign LMS is used for implementaiion

$$g_i[n+1] = g_i[n] + \mu \,\mathrm{sign}(e[n])\,\mathrm{sign}(\frac{\partial e}{\partial g_i}) \tag{4.15}$$

Several calibration configurations are simulated for comparison, as shown in Figure 5.1. These include:

(a) Without calibration

(b) Gain-only calibration

(c) Bit-weight only calibration

(d) Combined bit-weight and gain calibration

(e) Combined bit-weight and nonlinearity calibration for both residue amplifiers

(f) Bit-weight calibration with nonlinearity calibration for the first RA and gain calibration for the second RA

We can see that the "gain-only" and "bit-weight-only" calibration only bring limited improvement. This is because when one of them is calibrated, the other one becomes the bottle-neck. When the bit-weight error and gain error are calibrated together. The SNDR and SFDR shows noticeable improvement. The best result is achieved when the nonlinearity calibration is applied, since it compensates for the amplifier nonlinearity that remains after gain correction. The configuration using nonlinearity calibration for the first amplifier and gain calibration for the second one achieves almost the same performance as applying nonlinearity calibration to both amplifiers, since inter-stage gain suppresses the effect of second-stage nonlinearity on the overall ADC output, so this configuration is finally adopted in this work.

Figure 4.6 shows the block diagram of the corresponding calibration scheme for the proposed three-stage pipelined ADC. The update functions are shown as 4.16.

$$\begin{cases} e[n] = D_{out}[n] - V_{in}[n] \\ \hat{g}_1[n+1] = \hat{g}_1[n] + \mu \,\mathrm{sign}(e[n])\,\mathrm{sign}(O_2) \\ \hat{h}_1[n+1] = \hat{h}_1[n] + \mu \,\mathrm{sign}(e[n])\, O_2^3 \\ \hat{g}_2[n+1] = \hat{g}_2[n] + \mu \,\mathrm{sign}(e[n])\,\mathrm{sign}((\hat{g}_1[n] + 3\hat{h}_1[n]O_2^2)O_3) \\ \hat{w}_1[3:0][n+1] = \hat{w}_1[3:0][n] + \mu \,\mathrm{sign}(e[n]) \cdot \,\mathrm{sign}(code_1[3:0][n]) \end{cases} \tag{4.16}$$

For $\hat{h}_1$, the sign LMS is used instead of sign-sign LMS, since using sign-sign LMS loses the amplitude information of the nonlinear term O_2^3, which could results in slower convergence or even divergence.

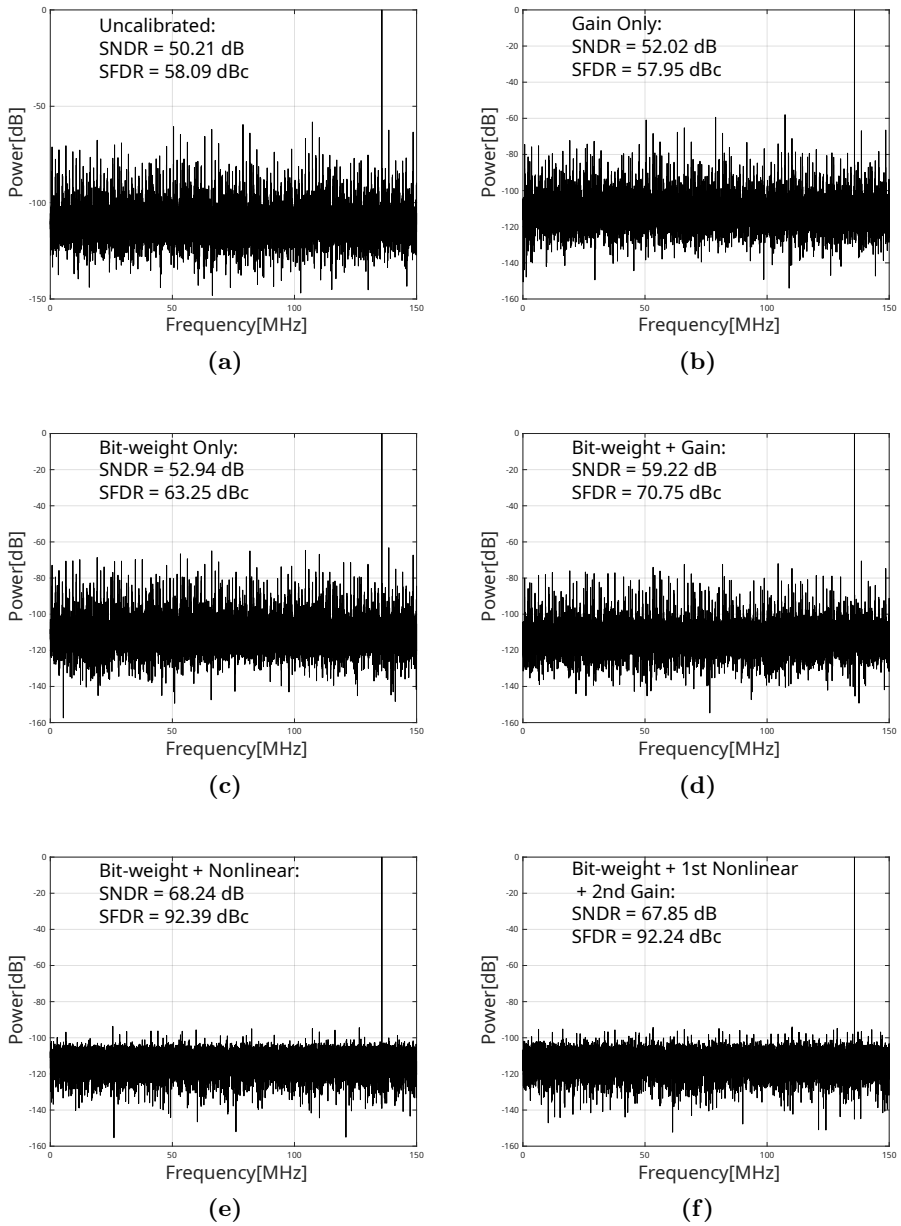


Figure 4.5: Performance with different calibration scheme(Behavior level)

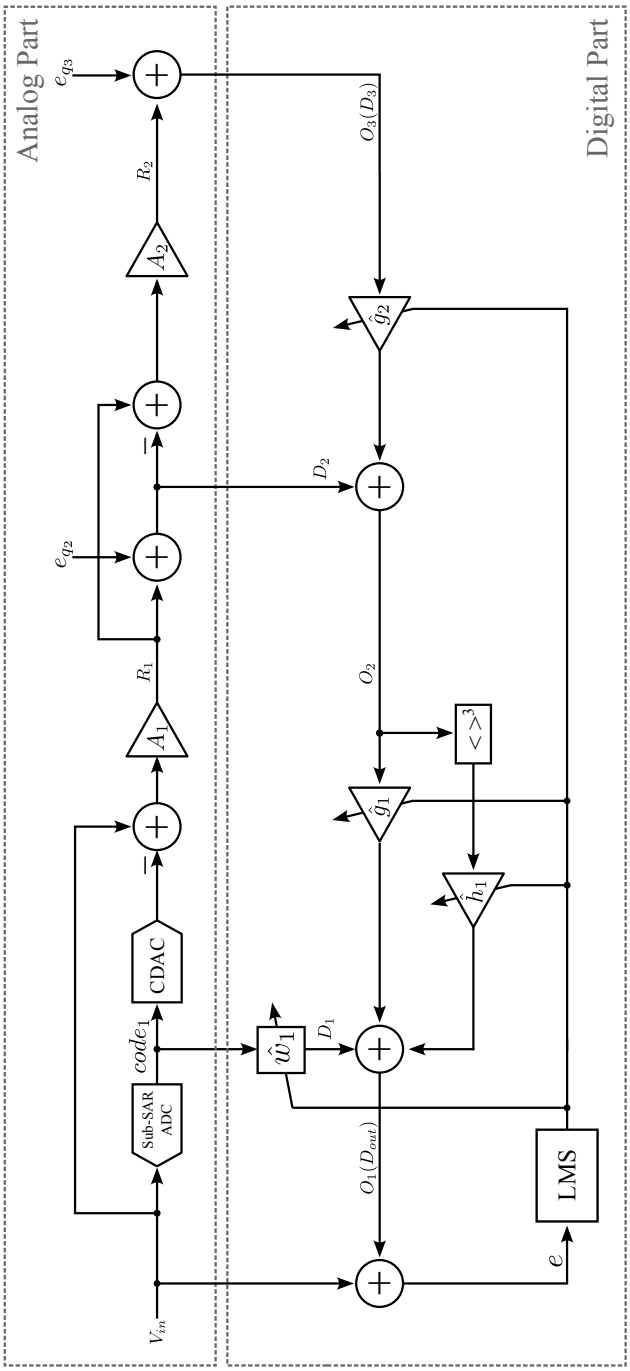


Figure 4.6: Block diagram of final adopted calibration scheme

Chapter 5
Simulation Results

The proposed pipelined Lu-SAR ADC is implemented at the transistor level, while the digital calibration part shown in Figure 4.6 is modeled in MATLAB. The digital outputs from transistor-level simulations are post-processed in MATLAB for calibration and performance evaluation.

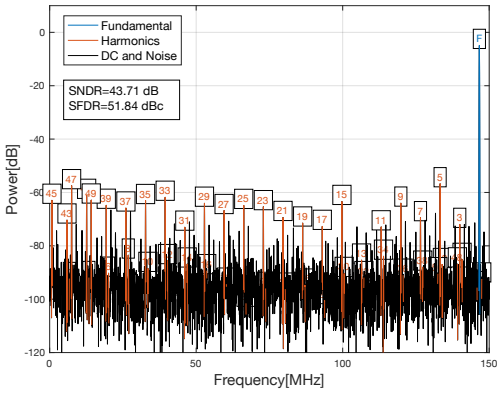
5.1 Performance under Different Calibration Schemes

Figure 5.1 shows the simulated output spectra under different calibration configurations with a Nyquist-rate differential input of 1.6 V peak-to-peak at the TT corner and a temperature of 40°C.

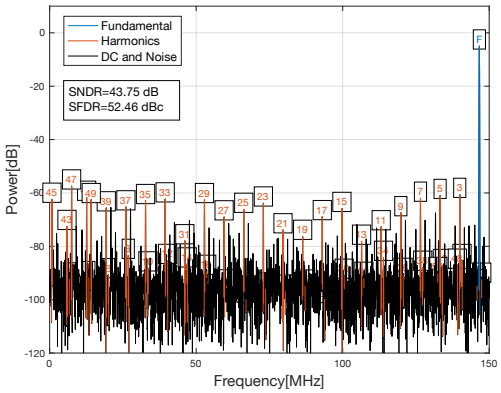
In the uncalibrated case, the two residue amplifiers are assumed to have fixed gains of 8 and 4, respectively, and the sub-ADCs use ideal binary bit weights. The SNDR and SFDR of the uncalibrated ADC are only 43 dB and 51 dB, respectively. Applying only bit-weight calibration or only gain calibration yields limited improvement, because calibrating one parameter exposes the other as the performance bottleneck, which is consistent with the results at behavior level. When both bit-weight and gain calibrations are applied, the performance of the proposed ADC improves significantly. Furthermore, with the nonlinear calibration for the first-stage amplifier, the SNDR and SFDR increase to above 60 dB and 80 dB, respectively.

5.2 Performance vs Input Signal Amplitude and Frequency

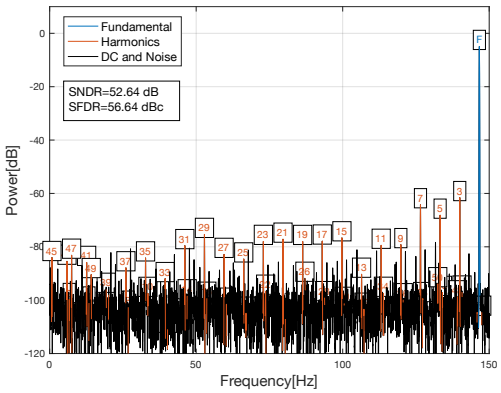
The SNDR and SFDR versus input amplitude and versus input frequency are plotted in Fig. 5.2 and Fig. 5.3, respectively. From the amplitude sweep, we can see that both SNDR and SFDR increase as the input amplitude becomes larger. When the input is small, the noise floor dominates, so the overall performance is limited. As the input amplitude moves closer to full scale, the harmonic components remain well controlled after calibration, and the linearity improves. For the frequency sweep, the results show that the performance is quite stable across different input frequencies within the Nyquist band. Both SNDR and SFDR vary only slightly when the input frequency changes.



(a) Without Calibration

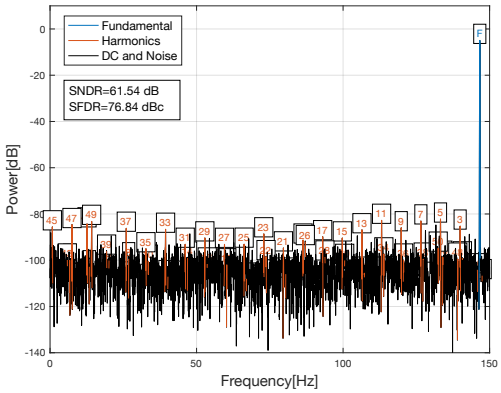


(b) With First Stage Bit-weight Calibration

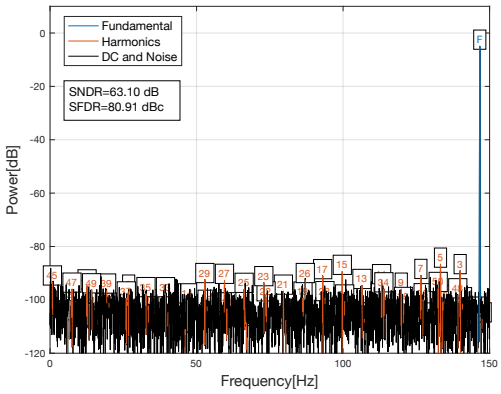


(c) With Gain Calibration

Figure 5.1: Output Spectrum with different calibration schemes(Part 1)



(d) With Bit-weight and Gain Calibration



(e) With Bit-Weight and Nonlinearity Calibration

Figure 5.1: Output Spectrum with different calibration schemes(Continue)

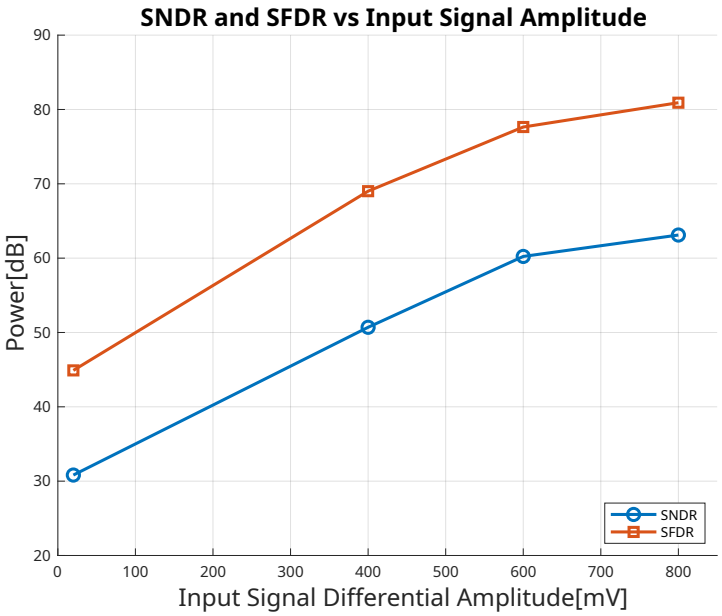


Figure 5.2: Performance vs Input signal amplitude

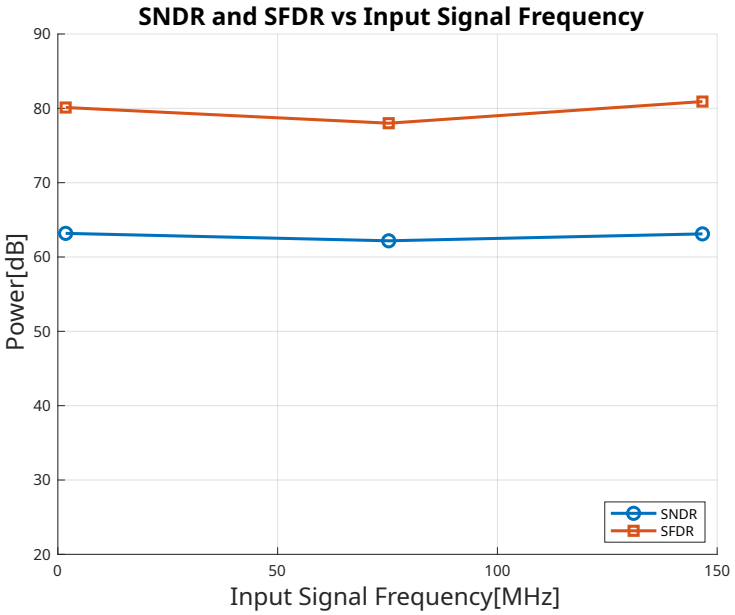


Figure 5.3: Performance vs Input signal frequency

5.3 Performance vs Temperature under Process corners

The SNDR and SFDR across temperature and process corners are shown in Figure 5.4 and Figure 5.5, respectively. In the TT corner, the performance remains stable at low and medium temperatures, but drops noticeably at high temperature. In the SS corner, the degradation becomes more significant, while the FF corner shows relatively small variation. The performance degradation under SS corner and high temperature is manly because of the increasing resistance of the RC sampling network.

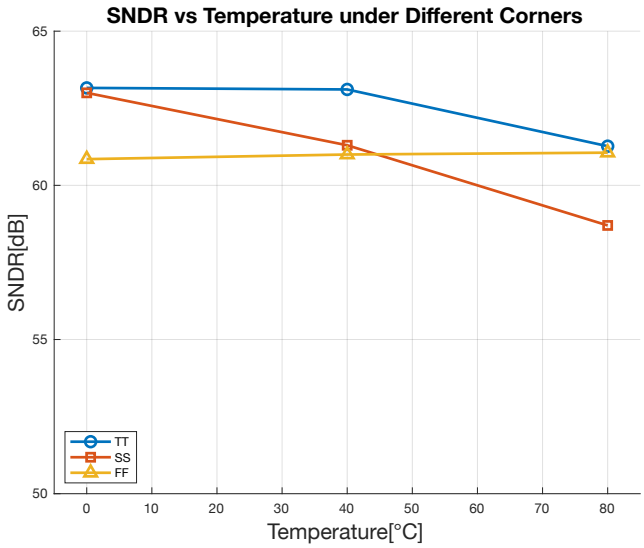


Figure 5.4: SNDR vs Temperature under Different Corners

5.4 Power Consumption

The power consumption of the proposed ADC is summarized in 5.1. It shows that the first residue amplifier (RA1) dominates the total power consumption. This is because it must operate at high speed while maintaining sufficient accuracy to meet the precision requirement of the following stages. Moreover, RA1 adopts a two-stage amplifier topology, and its second stage operates with a higher supply voltage to ensure sufficient output swing, which further increases its power consumption.

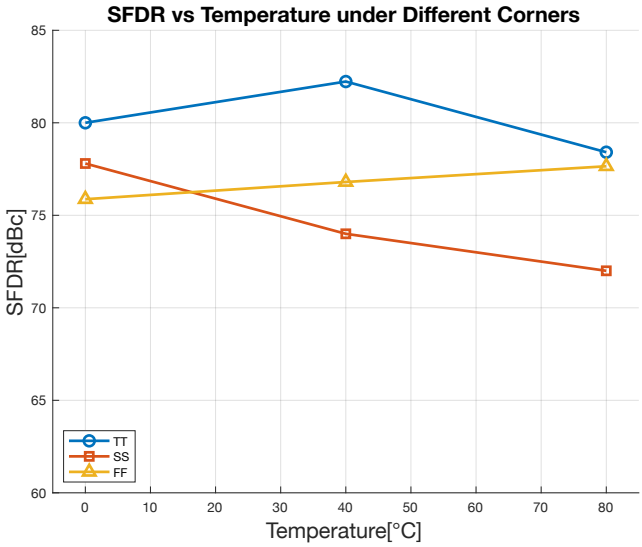


Figure 5.5: SFDR vs Temperature under Different Corners

	Power[mW]
RA1	7.3
RA2	1.7
SAR Total	1.8
Total	10.8

Table 5.1: Power consumption of proposed ADC

Chapter 6
Future work and Conclusion

6.1 Future Work

There are still several directions that can be explored in future work.

First, the proposed ADC is only implemented at the transistor level. The layout and post-layout simulation should be completed, especially the routing parasitics around the CDAC and the residue amplifiers, which may affect settling and linearity.

Second, the calibration algorithm is now modeled in MATLAB at a behavioral level. A hardware implementation is still needed. This includes choosing the proper word length, checking the fixed-point accuracy, and designing a reasonable update step to make sure the LMS works. In additon, a dither-based calibration method can be explored to avoid the using of reference ADC as well.

Third, the CMFB in the residue amplifier is fully passive and does not use any reference voltage. Because of this, the output common-mode voltage can shift under different process corners, especially in SF and FS corners. A common-mode compensation technique can be added in future work to stabilize the common-mode level.

Overall, future work should focus on completing the full IC implementation and improving the robustness of the calibration and amplifier design under PVT variations.

6.2 Conclusion

This thesis presents the design and analysis of a three-stage pipelined Lu-SAR ADC in 65 nm CMOS. The main non-idealities in the system, including sampling distortion, comparator offset, capacitor mismatch, and the gain and nonlinearity of the open-loop residue amplifiers, are analyzed. To improve accuracy, an LMS-based background calibration is developed, which can correct bit-weight error, gain error, and the nonlinear term of the first residue amplifier.

The transistor-level simulations, together with MATLAB post-processing, show that the proposed ADC can achieve above 60-dB SNDR and around 80-dBc SFDR at 300 MS/s after calibration. The results indicate that combining simple open-loop amplification with digital calibration can still provide good linearity under limited power budget.

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