Popular Science Summary

In an increasingly connected world, the demand for fast wireless communication, like 5G and 6G, is rapidly growing. To process these wireless signals, our devices heavily rely on a crucial mathematical algorithm called the discrete Fourier transform (DFT). However, traditional computers have an architectural limit. They suffer from the *von Neumann bottleneck*, which means they waste massive amounts of time and energy simply moving data back and forth between the memory unit and the processing unit.

A solution to overcome this bottleneck is to perform the calculations directly inside the memory itself. This can be achieved with the emerging devices called *memristors*. Arranging these analog components in a grid-like structure called a crossbar array, we can utilize the current flowing through it, to do math directly inside the arrays. Using this can drastically reduce time complexity and save power.

In this project, our main purpose was to simulate and evaluate the best way to build a DFT calculator using these memristor crossbars. We proposed and tested three different hardware designs:

- Baseline: A standard, straightforward implementation of the DFT using differential pairs.
- Merged: A design where we stacked the calculation matrices together to significantly reduce the hardware cost of expensive peripherals, like analog-to-Digital Converters (ADCs).
- Symmetry: A highly optimized design that leverages the natural mathematical symmetry of the DFT to cut the required crossbar area completely in half for real-valued inputs.

Using a modified NeuroSim simulator, we found our Symmetry design consumes only 8.65 nJ of energy. This is roughly half the energy required by highly optimized traditional hardware setups. However, scaling up to larger computations (like a 1024-point DFT) introduces a major challenge known as *IR drop*. This phenomenon is linked to the natural resistance of longer interconnecting wires, causing a voltage loss that heavily degrades calculation accuracy.

To mitigate this IR drop, we introduce *tiling* to break the massive crossbar into smaller, interconnected grids. Furthermore, because adding tiles requires expensive extra peripherals (like the previously mentioned ADCs) that increase

energy and area costs, we performed a tradeoff analysis. We found that a square tile size of 1024 offers the most optimal balance between energy efficiency and accuracy for a 1024-point DFT.