LO Generation and Frequency Division at mm-Wave and Sub-Terahertz Frequencies

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LO Generation and Frequency Division at mm-Wave and Sub-Terahertz Frequencies

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Abstract

This Thesis presents the design and investigation of high-frequency fundamental VCO(Voltage controlled oscillator) and injection-locked frequency dividers (ILFDs) for millimeter-wave (mmWave) and sub-terahertz (sub-THz) communication systems. A magnetically tuned voltage-controlled oscillator (VCO) and magnetically tuned ILFD pair are proposed for sub-THz applications. The 140 GHz fundamental VCO achieves a phase noise of -100.6 dBc/Hz at 10 MHz offset with a figure-of-merit (FOM)-178 dBc/Hz at 10 MHz with a tuning range of 6.43 %. while the ILFD covers 133–154.5 GHz with a locking range of 18.12 % and total power consumption of the pair is 7.2 mW. Additionally, a 200 GHz divide-by-two ILFD is demonstrated, covering 186.5–224.5 GHz with a locking range of 19.34 % and consuming 4.2 mW. The circuits operate with a 1.2 V supply and are implemented in a 65 nm CMOS process, with simulations conducted in Cadence Virtuoso. The limitations of the current design and potential improvements are discussed, highlighting its applicability for future 6G mmWave and sub-THz transceivers.

Popular Science Summary

At the heart of future wireless systems such as 6G lies the push toward extremely high frequencies, extending into the sub-terahertz (sub-THz) and terahertz (THz) range. These frequencies promise ultra-high data rates and the ability to support emerging applications such as immersive communication and high-resolution sensing. However, moving to such high frequencies is not just a simple extension of today's radio technology—it introduces a completely new set of challenges. At lower frequencies, such as sub-6 GHz and even millimeter-wave bands, modern transceivers rely on well-established architectures that combine amplifiers, mixers, and local oscillators to transmit and receive signals efficiently. As frequencies approach the THz range, these conventional approaches begin to break down. Semiconductor devices struggle to provide sufficient gain, power efficiency drops, and noise performance degrades significantly. As a result, signals attenuate quickly, limiting communication distances unless advanced techniques are used. In particular, ultramassive numbers of antenna elements must be combined coherently with sharp beamforming, with thousands to tens of thousands of antenna elements potentially required for THz base stations. One of the key challenges in these systems is the generation of stable and low-noise signals at extremely high frequencies. Instead of distributing a single high-frequency signal across a chip—which would consume excessive power—engineers increasingly rely on distributed architectures, where many local oscillators operate in parallel. This approach improves scalability but also introduces new challenges, such as maintaining coherence and controlling phase noise across the system.

This thesis focuses on addressing some of these challenges through the design of a sub-THz voltage-controlled oscillator (VCO) and an injection-locked frequency divider (ILFD). The VCO is responsible for generating high-frequency signals, while the ILFD enables efficient frequency scaling and improved phase noise performance. By carefully designing these building blocks, it becomes possible to generate and manipulate high-frequency signals more efficiently, which is essential for future large-scale systems. The work contributes to ongoing efforts to make sub-THz and THz communication systems practical. While significant challenges remain, advances in circuit design—such as the techniques explored in this thesis—are key steps toward realizing the high-speed, high-capacity wireless networks envisioned for the next generation of communication technologies.

Acknowledgments

First and foremost, I would like to express my gratitude to my supervisor, Henrik Sjöland, for his guidance, valuable feedback, and for enabling me to carry out my thesis within the EIT department. I would also like to thank Iman Ghotbi for providing helpful tips throughout the project.

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Abbreviations

PLL	Phase-Locked Loop
CML	Current Mode Logic
ILFD	Injection-Locked Frequency Divider
VCO	Voltage-Controlled Oscillator
LO	Local Oscillator
ACLR	Adjacent Channel Leakage Ratio
EVM	Error Vector Magnitude
mmWave	Millimeter-Wave
CMOS	Complementary Metal-Oxide-Semiconductor
FD-SOI	Fully Depleted Silicon-On-Insulator
PD	Phase Detector
LPF	Low-Pass Filter
ADS	Advanced Design System
PDK	Process Design Kit
FoM	Figure of Merit
FoM$_T$	Figure of Merit with Tuning Range

Chapter 1
Introduction

The rapid growth of mobile data traffic has pushed wireless systems toward millimeter-wave (30–100GHz) and sub-terahertz (100–300GHz) frequencies to enable multi-gigabit and even terabit-per-second data rates. Operating at such high frequencies imposes stringent requirements on local oscillator (LO) generation. The LO provides the reference for upconversion and downconversion, and its phase noise, stability, and accuracy directly impact system metrics such as EVM, and ACLR

Most transceivers employ a phase-locked loop (PLL) for frequency synthesis. The PLL multiplies a stable low-frequency reference—typically derived from a crystal oscillator—to the desired carrier frequency. The voltage-controlled oscillator (VCO) within the PLL generates the output frequency and is therefore the dominant contributor to phase noise. At mmWave frequencies, VCO design becomes difficult due to limited transistor gain (reduced Fosc/Fmax ratio), increased parasitic effects, and higher losses in passive components. As frequency increases, phase noise typically worsens because noise scales with frequency multiplication, and device noise contributions become more pronounced.

Frequency dividers are critical in PLLs and for quadrature LO generation. At mmWave, high-speed dividers like ILFDs, CML dividers, or regenerative dividers are used, balancing power, locking range, and phase accuracy. At sub-THz, sustaining oscillation and maintaining signal integrity is harder, often requiring distributed or coupled oscillator arrays and injection-locked or regenerative dividers.

In summary, low phase noise, wide tuning range, low power, and high-speed division are central challenges for mmWave and sub-THz LO design, and careful co-design of VCOs, PLLs, and dividers is essential for next-generation 5G and future 6G systems.

1.1 This thesis

This thesis was conducted at the Department of Electrical and Information Technology, Lund University, Sweden. The overall objective was to investigate fundamental local oscillator (LO) generation and frequency division for mm-wave and sub-terahertz applications. The scope of this work was limited to the high frequency components, highlighted in gray as shown in Fig 1.1, with a particular focus on locking range and tuning range.

All circuit simulations were performed using Cadence Virtuoso, while electromagnetic simulations of the inductors were carried out using Keysight Momentum. The designs were implemented

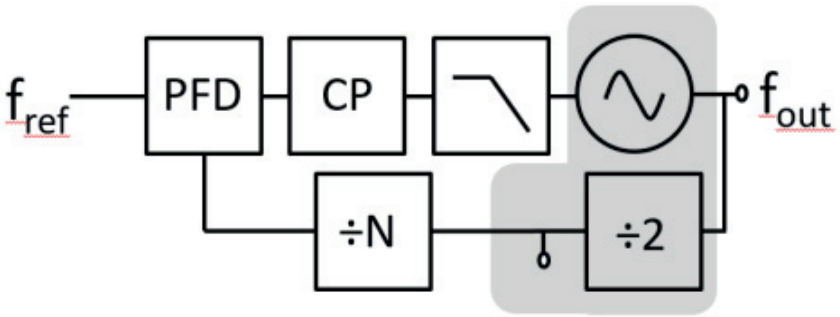


Figure 1.1: PLL architecture

in a 65 nm bulk CMOS technology, operating from a 1.2 V supply voltage.

1.2 Report organization

The thesis is organized as follows:

- **Chapter 2:** A brief introduction of PLLs.
- **Chapter 3:** Basics of an LC oscillators and injection locking for frequency division.
- **Chapter 4:** Implementation of inductors at mm-Wave frequency.
- **Chapter 5:**mmWave VCO and ILFD.
- **Chapter 6:** Sub-terahertz VCO and ILFD; 200GHz Divide-by-2 is presented.
- **Chapter 7:** Future work and Conclusion.

Chapter 2

Phase-Locked Loops

A phase locked loop (PLL) is a feedback loop widely used for clock generation and frequency synthesis in communication systems. It synchronizes the output of a voltage-controlled oscillator (VCO) with a high-precision reference signal so that both signals remain phase aligned. This is achieved through negative feedback by continuously comparing the phase difference between the reference signal fref and the divided VCO output. A typical PLL consists of a phase detector (PD), loop filter (LF), VCO, and a frequency divider (÷N) in the feedback path as shown in Fig 2.1. The reference frequency, usually generated by a crystal oscillator, is compared with the divided VCO output in the phase detector, which produces a voltage proportional to the phase error. This signal is filtered by the loop filter and applied to the VCO to adjust its oscillation frequency.
When the phase error becomes constant, the PLL is said to be locked, meaning the frequencies of the reference and divided signals are equal [1]. Since the divided signal is fs=fout/N, the output frequency of the PLL is given by

$$f_{out} = N \cdot f_{ref} \tag{2.1}$$

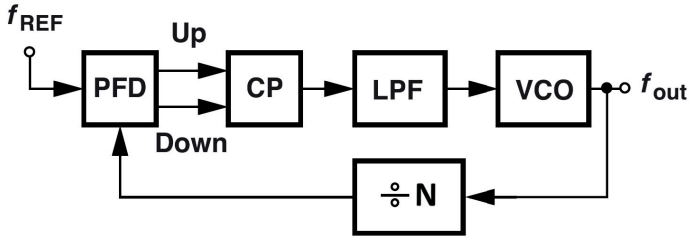


Figure 2.1: Block Diagram of CP-PLL [1]

PLLs are widely used in communication systems for carrier synchronization, carrier recovery, frequency division, frequency multiplication, and demodulation. The main design considerations include phase noise, RMS jitter, power consumption, reference spurs, and tuning range.

2.1 CP-PLL

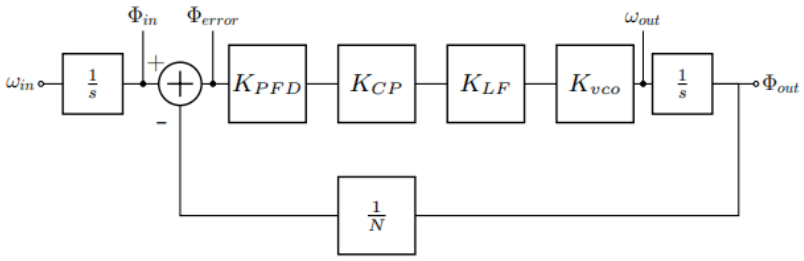


Figure 2.2: The mathematical representation of Charge pump PLL [32]

A phase-locked loop (PLL) is a feedback system used to synchronize the frequency and phase of a voltage-controlled oscillator (VCO) to a reference signal. The input to the PLL is a reference signal with frequency ω_{in} and phase Φ_{in}. The phase detector compares the reference phase with the feedback signal from the VCO output and generates a phase error Φ_{error} as shown in the above Fig 2.2. This error signal is converted into a voltage with gain K_{PD} and further processed by the charge pump and loop filter. The loop filter is characterized by the transfer function K_{LF} and produces a control voltage that tunes the VCO.

The VCO converts the control voltage into an output frequency according to its gain K_{VCO}, typically expressed in (rad/s)/V. Since phase is the integral of frequency, the VCO introduces an integrator in the loop, resulting in a transfer function proportional to K_{VCO}/s [2]. In a frequency synthesizer, the VCO output is divided by a programmable divider with ratio N before being compared with the reference signal. The resulting output frequency is therefore

$$f_{out} = N \cdot f_{ref} \tag{2.2}$$

By adjusting the divider value N, the PLL can generate different output frequencies with a resolution equal to the reference frequency f_{ref}. For higher frequency resolution, a Fractional-N architecture can be used where the divider ratio is modulated between different integer values to obtain a fractional average value..

The loop filter plays an important role in determining the stability and noise performance of the PLL. In its simplest form, the filter can be modeled as a constant gain, resulting in a first-order PLL. However, practical PLLs typically employ second-order or higher-order loop filters to eliminate steady-state phase error and improve noise filtering.

Another important parameter is the loop bandwidth. A wider bandwidth allows faster locking and reduces the impact of VCO phase noise within the loop bandwidth. However, excessively large bandwidths reduce filtering of noise on the control voltage and may introduce instability due to the

sampled nature of the phase detector. Therefore, the loop bandwidth is commonly chosen to be less than approximately 10% of the reference signal.

In terms of noise behavior, the PLL acts as a low-pass filter for phase noise originating from the reference and other preceding blocks, while it behaves as a high-pass filter for phase noise generated by the VCO. Consequently, minimizing the in-band noise contributions from the phase detector, charge pump, and loop filter is essential for achieving low overall phase noise.

Chapter 3

Oscillators and Injection locking

3.1 Oscillator

The LC-oscillator uses the resonance frequency of an LC-tank circuit to provide the positive feedback required for sustaining oscillations. There are many different structures such as the tuned collector/base, Hartley, Colpitts, Clapp, cross-coupled, etc. For integrated radio applications, the cross-coupled LC oscillator is the most attractive one. A common LC-tank VCO consists of an LC tank, a frequency tuner, cross-coupled transistor pair, and a tail current source as shown in the below Fig 3.1.

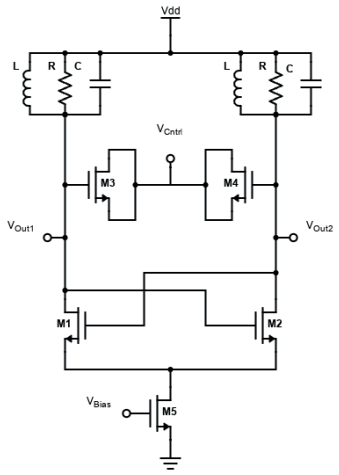


Figure 3.1: LC-VCO

According to the Barkhausen criterion, for sustained oscillations, a circuit will sustain stable oscillations only for frequencies at which the loop gain of the system is equal to 1 and the phase

shift between input and output is 0 or integral multiples of an integral multiple of 2π.
The resonance frequency is given by

$$\omega = \frac{1}{\sqrt{LC}}$$

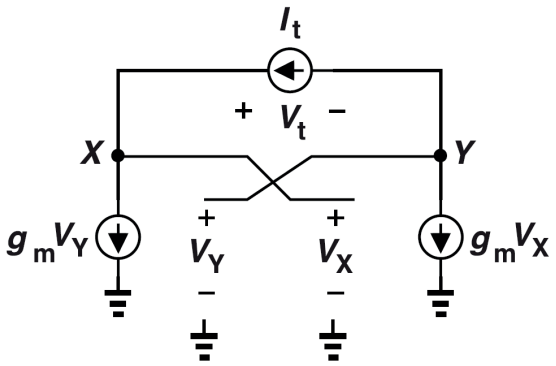


Figure 3.2: Equivalent circuit of LC-VCO for calculation[1]

The cross-coupled transistor pair is used to generate negative resistance which as be calculated as shown in Fig 3.2. Oscillators operating based on this principle are commonly referred to as negative-resistance oscillators which is

$$\frac{i_t}{V_t} \approx -\frac{g_m}{2} \tag{3.1}$$

which represents a negative resistance. If this negative resistance is designed to cancel the positive parasitic resistance in the LC tank, sustained oscillation can be achieved, for small signals, the negative conductance should be greater than the conductance of the tank by e.g. a factor of 2-3 for robustness.

When the cross-coupled pair is included in the circuit, the oscillation frequency must be recalculated because the transistor parasitic capacitances increase the total capacitance of the resonator. So, the oscillation frequency is determined by the below expression

$$f_{\text{osc}} = \frac{1}{2\pi\sqrt{L\left(C + C_{db} + C_{gs} + 4C_{gd}\right)}} \tag{3.2}$$

where C_{db}, C_{gs}, and C_{gd} represent the parasitic capacitances of the cross-coupled pair [1]. Due to these additional parasitic capacitances, the oscillation frequency becomes lower than that of an ideal LC tank.

3.2 Voltage controlled Oscillator

3.2.1 Varactor

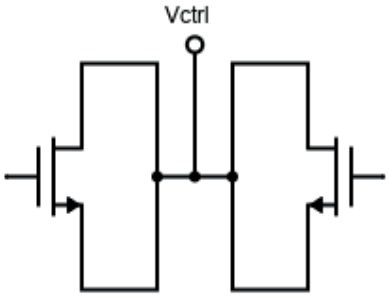


Figure 3.3: Varactor

A varactor enables an oscillator to be voltage controlled by providing a variable capacitance that changes the oscillation frequency as the applied voltage varies. The varactor as shown in Fig 3.3 is directly controlled by the signal from the output of the loop filter in the PLL. By varying the capacitance of the varactor, the total capacitance of the LC tank is modified, which results in a change in the oscillation frequency.

3.2.2 Magnetic Tuning

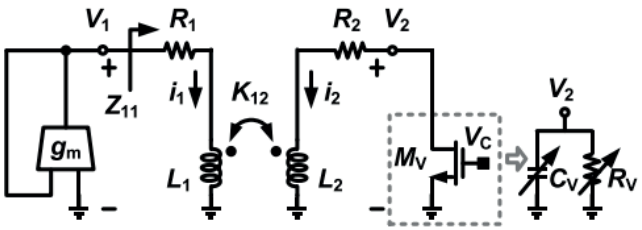


Figure 3.4: Conceptual View of Magnetic tuning

As the operating frequency approaches the sub-terahertz range, the losses associated with varactors become significant due to their very low Q-factor at such high frequencies. This degradation in Q-

factor adversely affects the oscillator performance. Therefore, magnetic tuning is adopted as an alternative approach to achieve frequency tuning.
The magnetic tuning of the oscillator can be realized through a two-coil transformer, where the resonant primary coil L_1 is connected to a negative transconductance (g_m) cell to sustain stable oscillation. A variable resistor R_V, is connected in parallel with the secondary coil L_2 for fine tuning as shown in Fig 3.4.

The current i_1 flowing through the primary coil L_1 generates a self-magnetic flux linkage, while the current i_2 in the secondary coil L_2 produces an additional flux through mutual coupling [3],[4],[5]; by adjusting the load impedance Z_V, the current i_2 can be controlled, which modifies the coupled magnetic flux. This interaction changes the effective inductance seen by the primary coil L_1, enabling frequency tuning.

3.3 Phase Noise

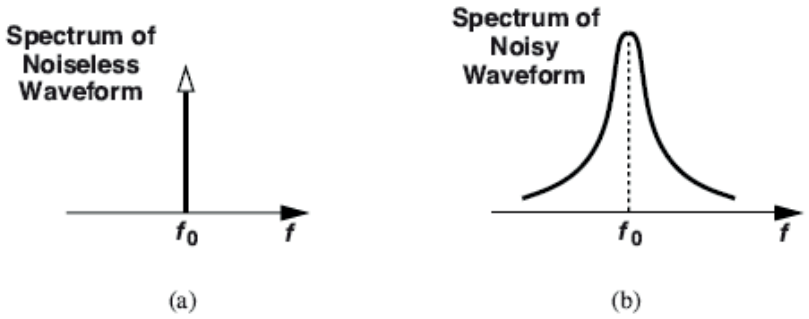


Figure 3.5: Spectra of sinusoidal waveform [1]

Ideally, an oscillator would generate a signal at a single frequency with an infinitesimally small spectral width. Such an oscillator would ensure that a transceiver neither interferes with nor is disturbed by nearby channels. In practice, however, this is not possible. Due to oscillator noise real oscillators produce a spectrum with a skirt-like shape centered around the resonance frequency, as shown in Fig. 3.5 b.

This spectral broadening is caused by random fluctuations in the oscillator phase and is referred to as *phase noise*. Phase noise can be considered a form of jitter originating from oscillators, but it is commonly analyzed in the frequency domain and treated as a separate parameter. In an ideal case, a single-frequency signal would appear as a spectral line with zero width as shown in Fig. 3.5 a. However, due to noise sources such as thermal noise, shot noise, and flicker noise, the oscillator spectrum spreads around the carrier frequency [1],[6].

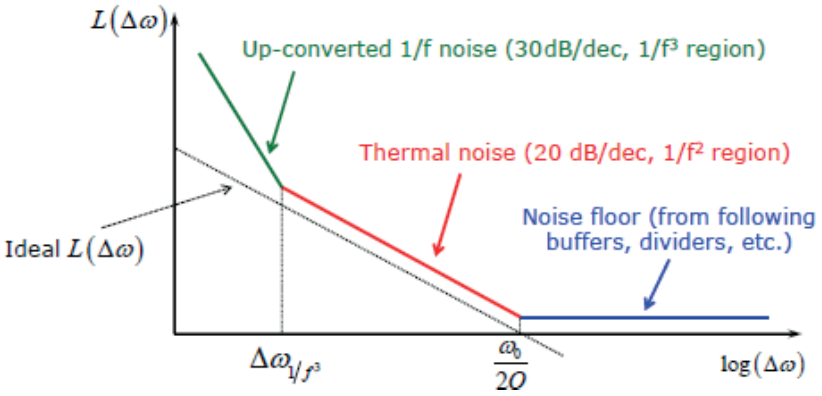


Figure 3.6: Oscillator Phase Noise in dBc/Hz vs. Frequency Offset [6]

Oscillator phase noise arises from both white thermal noise and low-frequency flicker noise of active devices. White thermal noise, originating from resistive elements and transistors, has a flat power spectral density $S_v(f) = 4kTR$ and induces instantaneous frequency deviations $\Delta\omega(t)$ in the oscillator. Since the oscillator phase is the integral of frequency deviations,

$$\phi(t) = \int \Delta\omega(t)\, dt,$$

the resulting phase noise power spectral density is

$$S_\phi(f) = \frac{S_{\Delta\omega}(f)}{(2\pi f)^2} \propto \frac{1}{f^2},$$

producing the characteristic -20 dB/decade slope in the medium-offset frequency region. Low-frequency flicker noise $(1/f)$ in the active devices is upconverted to the carrier frequency through the oscillator's nonlinear time-varying operation, resulting in a close-to-carrier $1/f^3$ phase noise slope with -30 dB/decade, while far-offset frequencies approach a flat noise floor $(1/f^0)$ as shown in Fig 3.6. Leeson's model [7] formalizes this behavior, predicting the single-sideband phase noise as

$$L(\Delta f) = 10\log_{10}\left[\frac{2FkT}{P_0}\left(1 + \frac{\omega_{1/f^3}}{\Delta\omega}\right)\left(1 + \left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right)\right]$$

where F is the oscillator noise factor, P_0 is the signal power in the resonator, Q is the resonator quality factor, ω_{1/f^3} is the flicker noise corner frequency, and $\Delta\omega$ is the offset from the carrier. From this it is clear that the resonator Q-factor and resonator signal power have to be maximized in order to minimize the phase noise.

3.4 Injection Locking

To establish steady-state oscillation without signal injection, the Barkhausen criterion must be satisfied, requiring the loop gain to be unity and the total phase shift around the loop to be an integer multiple of 2π. In a cross-coupled LC oscillator, each transistor in the differential pair (M_1 and M_2) contributes a phase shift of π, and therefore the LC tank must provide zero phase shift. This condition occurs at the resonant frequency $\omega_0 = 1/\sqrt{LC}$, where the magnitude of the tank impedance reaches its maximum value.

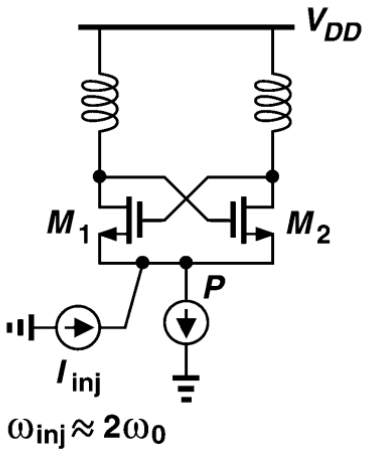


Figure 3.7: Injection locking in oscillator [8]

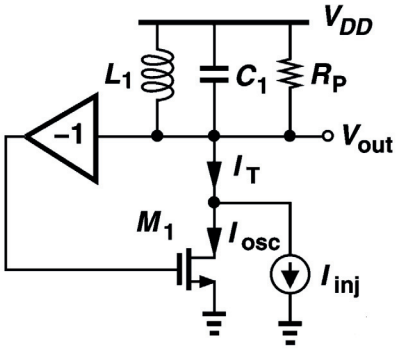


Figure 3.8: Equivalent circuit for Injection locking in oscillator [8]

Nxow consider an injection signal I_{inj} with phase difference ϕ_{inj} relative to the oscillator outputs (V_O^+ and V_O^-) is injected as shown in Fig 3.8. The current i_{osc} generated by M_1 is superposed with the injected current I_{inj}, producing a total tank current i_T with a phase shift of ϕ_O as shown in Figure 3.9. In order to satisfy the phase condition of the Barkhausen criterion, the LC tank must provide a compensating phase shift of $-\phi_O$. Since the LC tank can only provide phase shift when operating away from resonance, the oscillation frequency shifts from the natural resonance ω_0 to a new value ω [8],[9],[10].

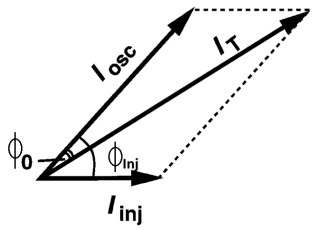


Figure 3.9: Equivalent circuit for Injection locking in oscillator [8]

Near resonance, the phase response of the LC tank can be approximated as

$$\theta(\omega) \approx 2Q\frac{\omega - \omega_0}{\omega_0},$$

where Q is the tank quality factor and ω_0 is the resonant frequency. To compensate the phase

perturbation introduced by the injected signal, the tank must satisfy

$$\phi = 2Q\frac{\omega - \omega_0}{\omega_0}.$$

The injected current i_{inj} combines with the oscillator current i_{osc}, introducing a maximum phase shift that can be approximated by

$$\sin\phi = \frac{i_{inj}}{i_{osc}}.$$

For small phase angles, $\sin\phi \approx \phi$, yielding

$$\omega - \omega_0 = \frac{\omega_0}{2Q}\frac{i_{inj}}{i_{osc}}.$$

Thus, the maximum locking range of the injection-locked oscillator can be expressed as

$$\Delta\omega_{lock} = \frac{\omega_0}{2Q}\frac{i_{inj}}{i_{osc}}.$$

3.5 Injection Locked Frequency divider

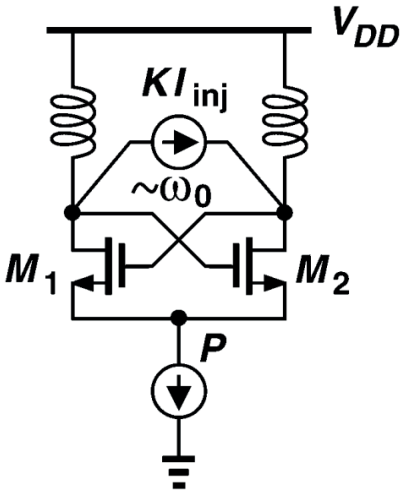


Figure 3.10: Injection Locked Divider [8]

Switching at a rate equal to the oscillation frequency ω_0, the M_1, M_2 transistors behave as a mixer that translates the injected signal at ω_{in} to frequency components at $\omega_{in} \pm \omega_0$ as shown in Fig

3.7. Due to the selectivity of the LC tank, the sum component is suppressed while the difference component appears near the oscillation frequency. Thus injection is equivalent to injection of kI_{inj} (where k is the mixer conversion gain) directly into the oscillator as shown in Fig 3.10. If the switching devices operate abruptly(Square wave), then $K = 2/\pi$, and the locking range expression can be written accordingly[8].

For a conventional injection-locked oscillator, the locking range can be expressed as

$$\Delta\omega = \frac{\omega_0 K}{2Q}\frac{I_{inj}}{I_{osc}}.$$

For a divide-by-two injection-locked frequency divider, the locking range referred to the input frequency must be doubled because the oscillator operates at half the input frequency. Hence, the input-referred locking range becomes

$$\Delta\omega_{in} = 2\Delta\omega.$$

3.5.1 Tail Injection

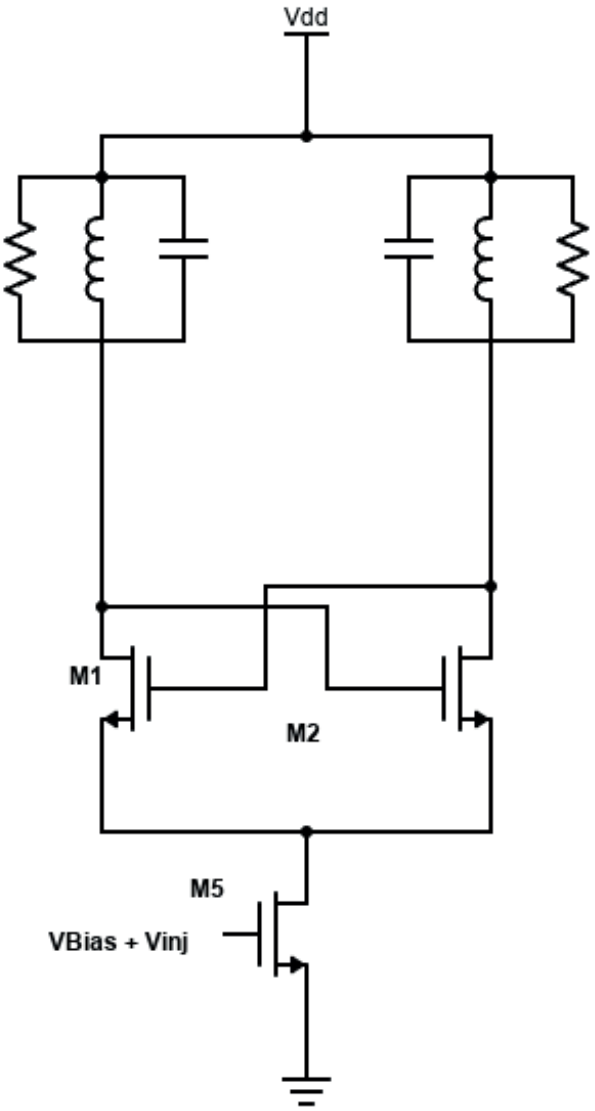


Figure 3.11: Divide-by-2 ILFD

A conventional approach for achieving injection locking is to inject the second-harmonic signal at the gate node of the current-source transistor as shown in Fig 3.11. This method is referred to as indirect injection, since the injected signal modulates the tail current rather than directly interacting with the resonator. As a result, the injection efficiency is typically lower compared to direct injection techniques, which will be discussed in the following section [11].

3.5.2 Direct single injector

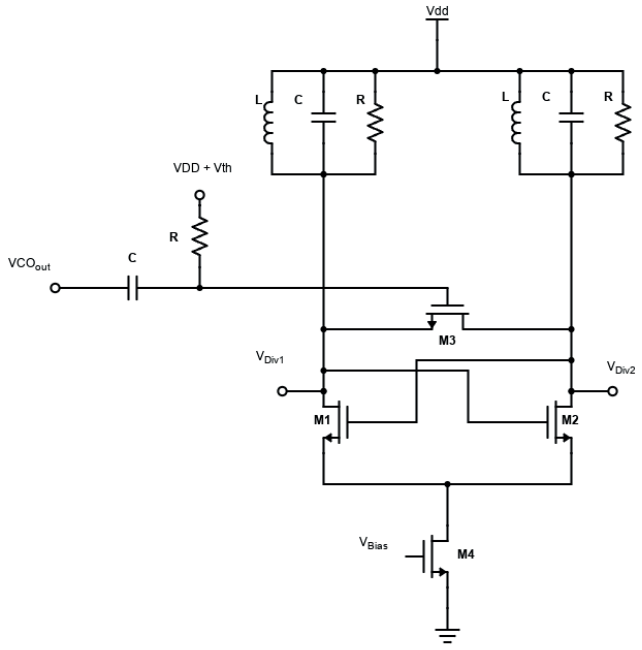


Figure 3.12: Divide-by-2 ILFD

A more efficient technique, known as direct injection , injects the signal at the gate of dedicated injection transistors placed between the differential output nodes of the ILFD as shown in FIg 3.12. But only one side of the differential VCO input swing is used [10].

3.5.3 Double injector

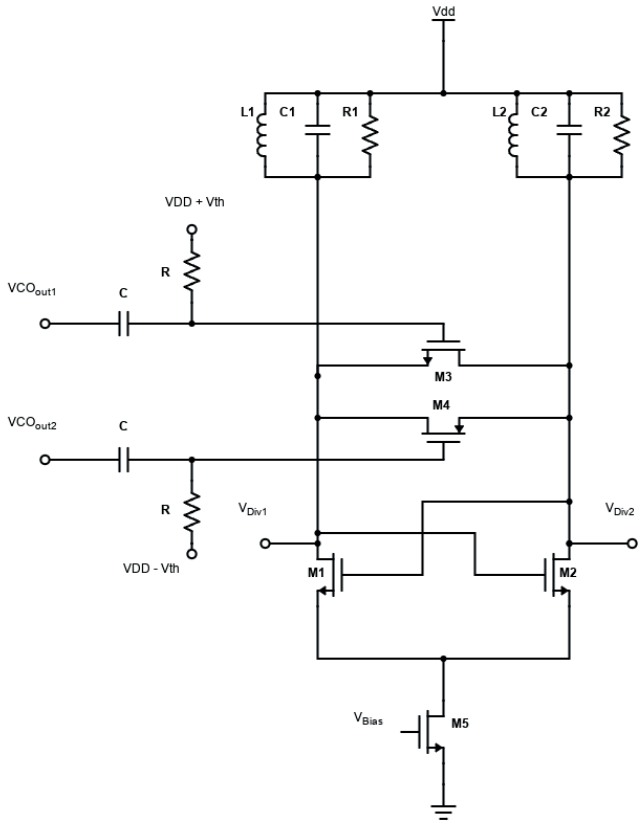


Figure 3.13: Divide-by-2 ILFD

In this approach, the operation is similar to direct injection, but the differential swing of the VCO is utilized as shown in Fig 3.13. This allows the circuit to take advantage of the full differential output swing of the VCO, thereby improving the injection efficiency. The injection transistors can be modeled as nonlinear mixers, and to maximize their conversion gain, their DC gate bias is carefully adjusted. Specifically, the NMOS gate voltage is biased approximately one threshold voltage above V_{DD}, while the PMOS gate voltage is biased approximately one threshold voltage below V_{DD}. This biasing condition enhances the mixing efficiency and strengthens the effective

injection current, leading to improved locking performance [12],[13].

3.5.4 Divide-by-3

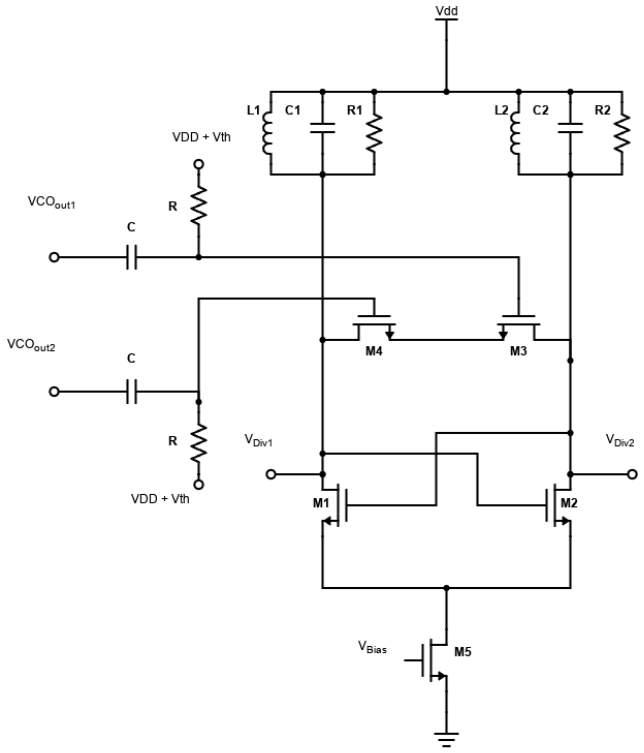


Figure 3.14: Divide-by-2 ILFD

The divide-by-3 injection-locked frequency divider (ILFD) consists of a differential LC oscillator core formed by the cross-coupled pair M_1 and M_2, a differential direct-injection pair, and a triode-based multiplier stage as shown in FIg 3.14. The differential injection transistors receive an RF input signal operating at approximately $3f_0$, while the LC tank is tuned to oscillate at f_0.

Due to the nonlinear behavior of the injection devices, the injected signal is mixed with the oscillator signal, producing harmonic and intermodulation components. Because the sources of the injection transistors are connected together, a common-mode signal is generated at the shared

source node, which further contributes to harmonic mixing.

The triode multiplier stage, implemented using transistors M_4 and M_5, multiplies the injected voltage at approximately $3f_0$ with the oscillator output at f_0. A MOS transistor operating in the triode region behaves as a voltage-controlled resistor, and its nonlinear current–voltage characteristic enables the mixing of the two signals. When driven by large (rail-to-rail) signals from the VCO, the stage effectively operates as a voltage-mode single-balanced mixer with differential input and single-ended output. The multiplication of signals at $3f_0$ and f_0 produces intermodulation components at

$$3f_0 \pm f_0 = 2f_0 \text{ and } 4f_0$$

as well as additional higher-order harmonic terms. The LC tank acts as a bandpass filter centered at f_0, suppressing undesired harmonics while reinforcing the frequency component that satisfies the locking condition [14],[15],[16].

Furthermore, frequency components around $2f_0$, $4f_0$, and other higher-order harmonics are also generated and coupled to the tail current device. The tail device behaves as a transconductance stage and injects current primarily at approximately $2f_0$ into the sources of the cross-coupled pair. This mechanism introduces an additional injection path similar to that of a divide-by-2 ILFD. At the same time, the injection pair also provides direct injection current at the fundamental harmonic to the output node.

As a result, the effective locking range of the divider is proportional to the combined contributions of both injection mechanisms. In the locked state, the nonlinear mixing continuously regenerates frequency components that sustain oscillation at f_0 while synchronizing the oscillator to the injected signal at $3f_0$. Consequently, the oscillator output frequency becomes exactly one-third of the injection frequency, thereby achieving divide-by-3 operation.

Higher locking ranges for such architectures have been demonstrated in advanced technology nodes, such as 28nm FDSOI[16].

3.5.5 Divide-by-4

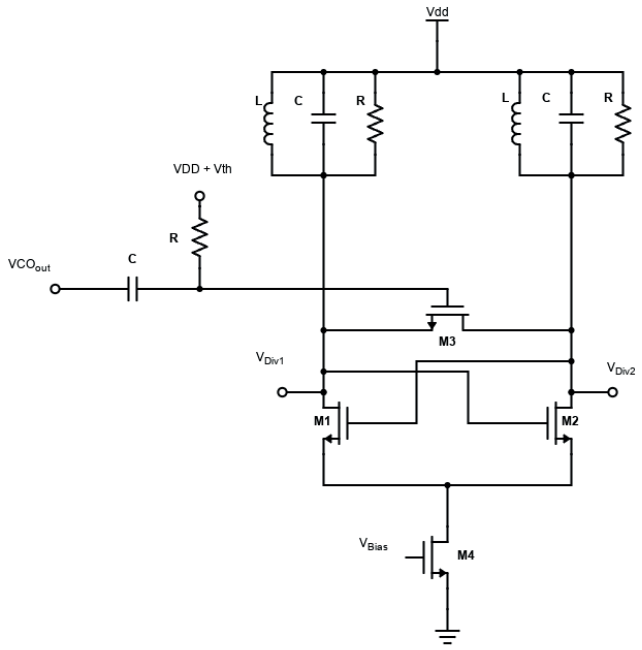


Figure 3.15: Divide-by-2 ILFD

For divide-by-4 operation, the injection transistor is forward body-biased to adjust its threshold voltage as shown in Fig 3.15. Similar to the divide-by-2 case with a single injector, the key difference here is that the injection transistor is biased in the subthreshold region, where the drain current follows an exponential relationship:

$$I_D \propto e^{\frac{V_{GS}}{nV_T}} \tag{3.3}$$

An optimal bias point can be found where the third-harmonic current component is maximized, which is essential for efficient divide by 4 injection locking. However, when the peak-to-peak swing of the VCO andor the ILFD is large, the injection transistor remains in the subthreshold region for only a small portion of the oscillation cycle. As a result, the effective third-harmonic current component decreases, leading to reduced injection efficiency and a smaller locking range. Therefore, a large signal swing does not necessarily improve injection efficiency in subthreshold-based harmonic injection[17].

In bulk CMOS technology, body biasing can be used to adjust the threshold voltage and optimize injection efficiency. However, applying forward body bias introduces junction leakage currents, which limits the extent to which the threshold voltage can be tuned. In contrast, FD-SOI technology provides improved flexibility because the body (back-gate) is electrically isolated from the substrate. This isolation allows the threshold voltage to be widely tuned using body bias without introducing significant junction leakage penalties. Consequently, FD-SOI offers superior control over the injection transistor biasing, enabling higher injection efficiency and potentially a larger locking range compared to bulk CMOS implementations.

In the available 65 nm CMOS PDK, a divide-by-4 ILFD with a center frequency of 55 GHz was designed, which achieves a free-running locking range of only 1.5 GHz without varactor tuning.

3.5.6 Higher Division ratios

Although higher division ratios such as divide-by-3 [18], divide-by-5 [19], divide-by-6 [20],[21], and beyond have been demonstrated, they generally exhibit a significantly smaller locking range. In practical systems, the divider must cover the full VCO tuning range while remaining robust against process, voltage, and temperature (PVT) variations. However, as the division ratio higher than divide-by-2 circuits, the effective harmonic injection strength decreases because higher-order harmonic components have smaller amplitudes and lower nonlinear conversion efficiency. Consequently, the achievable locking range shrinks, making these higher-ratio dividers less robust.

This limitation becomes even more critical at mm-wave and sub-terahertz frequencies, where device parasitics, reduced transistor gain, and limited voltage headroom further degrade injection efficiency. Therefore, although higher division ratios are possible, they are generally impractical for achieving wide tuning range coverage and robust operation in mm-wave and sub-THz frequency systems.

3.6 Figures-of-merit

The most established Figures-of-Merit (FoM) for the voltage controlled oscillator is :

$$\mathrm{FoM} = PN - 20\log_{10}\left(\frac{f_0}{\Delta f}\right) + 10\log_{10}\left(\frac{P_{\mathrm{DC}}}{1\ \mathrm{mW}}\right) \tag{3.4}$$

where PN is the phase noise given in dBc/Hz at a frequency offset Δf and P_{DC} is the power consumption of the oscillator.

The Figure-of-Merit above does not account for the tuning range, which is a another important merit for an oscillator. Therefore, another Figure-of-Merit that takes into account relative tuning range of VCO:

$$FoM_T = PN - 20\log_{10}\left(\frac{f_0}{\Delta f}\cdot\frac{TTR}{10}\right) + 10\log_{10}\left(\frac{P_{DC}}{1\,\mathrm{mW}}\right) \tag{3.5}$$

Here, TTR is the total frequency tuning range given in percent.

Unlike voltage-controlled oscillators (VCOs), there is no widely accepted figure-of-merit (FoM) for injection-locked frequency dividers (ILFDs) that comprehensively captures key performance

parameters such as power consumption, locking range, and tuning range. Therefore, ILFD performance is typically evaluated for a specified injection signal strength.

$$\text{Lock Range} = \frac{2(f_{max} - f_{min})}{f_{max} + f_{min}}$$

Chapter 4

Inductor Design

The implementation of inductors at mmWave frequencies and sub-terahertz is discussed. It should be noted that at the start of the thesis ADS was not available, so PDK inductors were used for mmWave designs upto 110GHZ(W-Band), For circuit nodes tuned to above 110GHz(D-band) ADS was used for inductor design.

The tank quality factor, the output swing, and the PN of the oscillator strongly depend on the inductor design. We focus on a single-turn octagonal structure, this shape provides two degrees of freedom, namely, the diameter, d, and the linewidth, W. The former defines the inductance, and the latter affects the loss. At millimeter- wave frequencies, the current tends to flow near the edges of the octagon due to skin effect, but W still plays some role in the inductor Q value [22] and self-resonance frequency.

4.1 Tuning at sub-terahertz Frequency

The main challenges of varactor tuning in the sub-terahertz frequency range is the low quality factor of the varactor as seen in fig 4.2. The Quality factor is measurement as shown in Fig 4.1. The low Q of the varactor loads the LC tank and degrades the overall quality factor of the resonator[23]. As a result, a larger cross-coupled transistor pair is required to generate sufficient negative resistance to start up and sustain oscillation. However, increasing the device size introduces additional parasitic capacitance, which in turn reduces the maximum achievable frequency of oscillation .

So we instead use magnetic tuning of Oscillator and ILFD at sub-terahertz. when using magnetic tuning the frequency tuning range increases with the coupling coefficient k, while the tank Q degrades with an increase in k. The coupling coefficient of the transformer can be varied by changing the space between the primary and secondary coils, which has a minimum space of 1.5 um with the designed technology if the same top metal M7 is used. By changing the space from 10 to 1.5 um in the used technology, the coupling coefficient simulated k varies from 0.249 to 0.488. Therefore, the coupling coefficient k between the two inductors used for magnetic tuning can be carefully chosen based on a trade-off between the resonator Q-factor, which affects the phase noise performance, and the achievable tuning range [24].

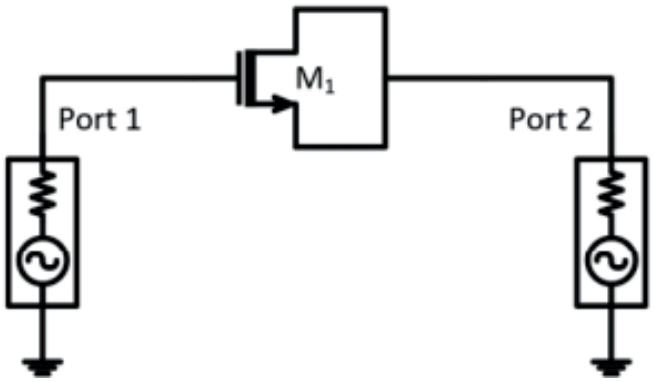


Figure 4.1: Simulation setup for Varactor testing [23]

4.2 Design of Transformers

For sub-terahertz VCO design, the inductor, which is a passive component of the LC tank, becomes one of the main limiting factors when attempting to achieve very high oscillation frequencies. To increase the oscillation frequency, the inductance must be reduced. One straightforward approach is to reduce the inductance by decreasing its inner diameter. However, aggressively reducing the inner diameter often leads to a significant degradation of the quality factor (Q-factor), which negatively affects the achievable oscillation frequency and particularly the phase noise. Therefore, the optimal inductor design should provide both a low inductance and a high Q-factor. As shown in the figure 4.3 (a) (b) below, the simulated inductance and Q-factor are plotted as a function of the width of the secondary (inner) inductor. Instead of reducing the outer diameter of the inductor from 47 μm to achieve a smaller inner diameter while keeping the trace width constant at 4 μm, the inductance can alternatively be reduced by increasing the trace width toward the inner turns. In this approach, the outer diameter is maintained at 47 μm, while the trace width is increased beyond 4 μm, resulting in a reduced inner diameter and, consequently, a lower inductance. As illustrated in the plot, this approach allows the inductance The inductance was reduced from 92.45 pH for a 4 µm metal width to 63.754 pH for an 8 µm metal width, while maintaining a relatively high Q-factor at 140 GHz. Consequently, the Inductor achieves a resonance frequency of 192 GHz with a 10 fF load capacitance, making it more suitable for high-frequency sub-terahertz VCO operation.

The designed transformers for the oscillators and dividers in this work are shown in figure 4.4, 4.5, and 4.6; along with their key geometrical and performance parameters in tables 4.1, 4.2, and 4.3. All the width are given in meters, inductance given in Henry. Sizing of inductors are presented; the 'w' indicates turn width, 'd' is the inner diameter, 'S' is spacing between two inductors, 'p' indicates primary inductor, 's' indicates secondary inductor.

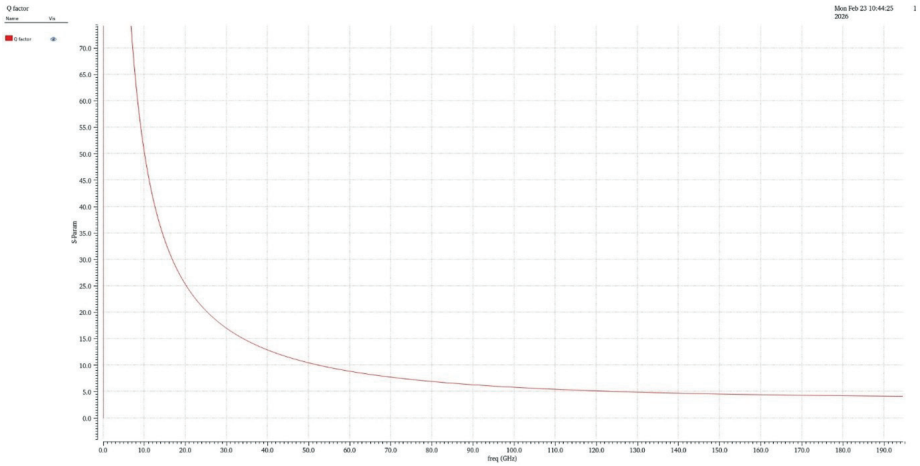
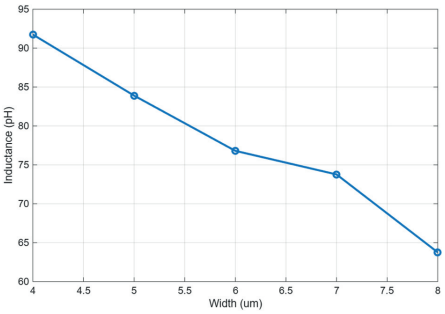
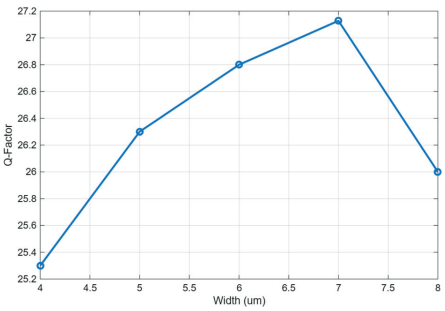


Figure 4.2: Simulated Q-factor of Varactor against frequency with W = 5um; L = 60nm



(a) Simulated Inductance vs Inductor Width at 140 GHz



(b) Simulated Q-factor vs Inductor Width at 140 GHz

Figure 4.3: Simulated characteristics of the inductor at 140 GHz.

4.2.1 140GHz VCO:

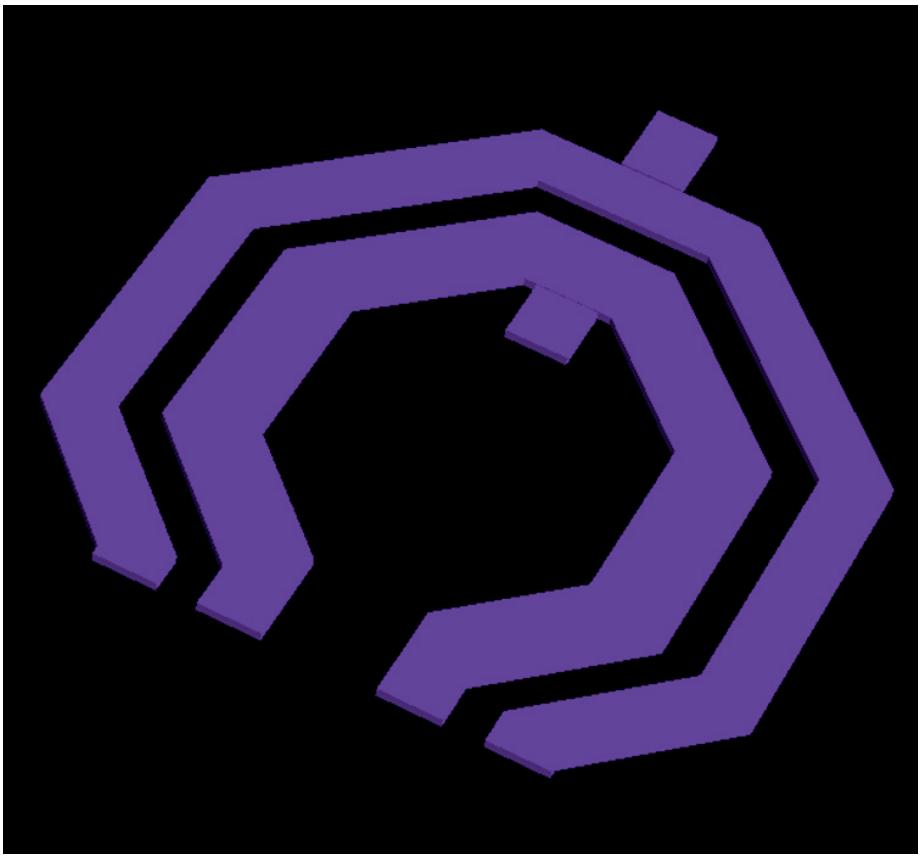


Figure 4.4: Designed Transformer for VCO

S.No	Parameters	Values
1	Lp	100p
2	Ls	63.754p
3	Qp	23
4	Qs	26
5	S	3.72u
6	Wp	5u
7	Ws	8u
8	K	0.42

Table 4.1: Design Parameters for D-Band VCO

4.2.2 140GHz Divide-by-2 ILFD:

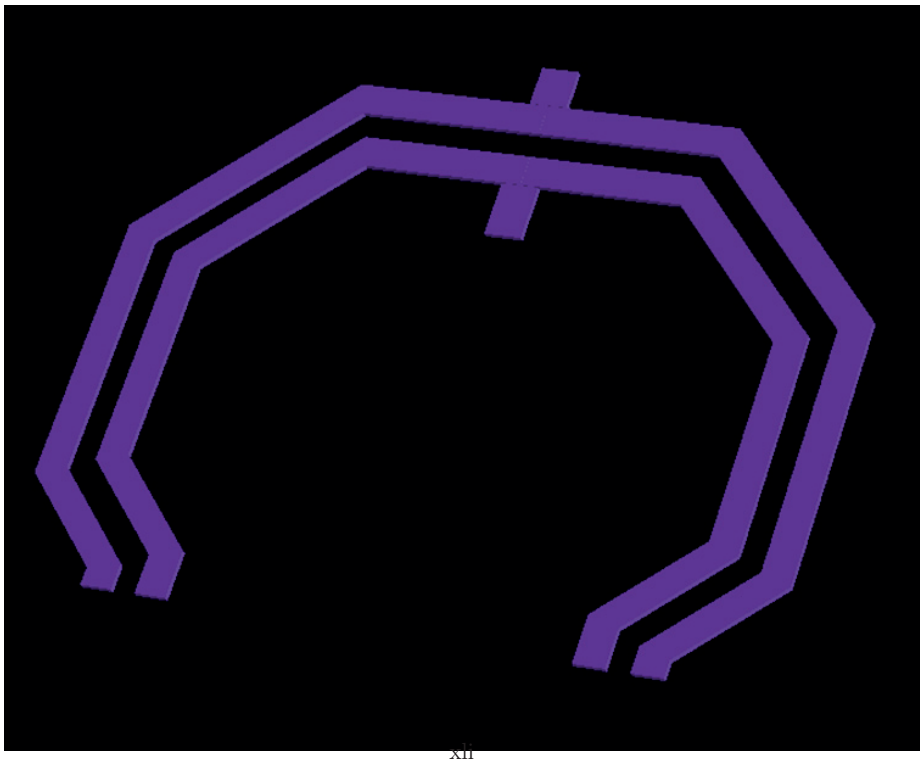


Figure 4.5: Designed Transformer for for D-Band Divide by 2 ILFD

S.No	Parameters	Values
1	Lp	158p
2	Ls	131p
3	Qp	25
4	Qs	26
5	S	4u
6	Wp,s	5u
7	K	0.473

Table 4.2: Design Parameters for D-Band Divide-by-2 ILFD

4.2.3 200GHz ILFD:

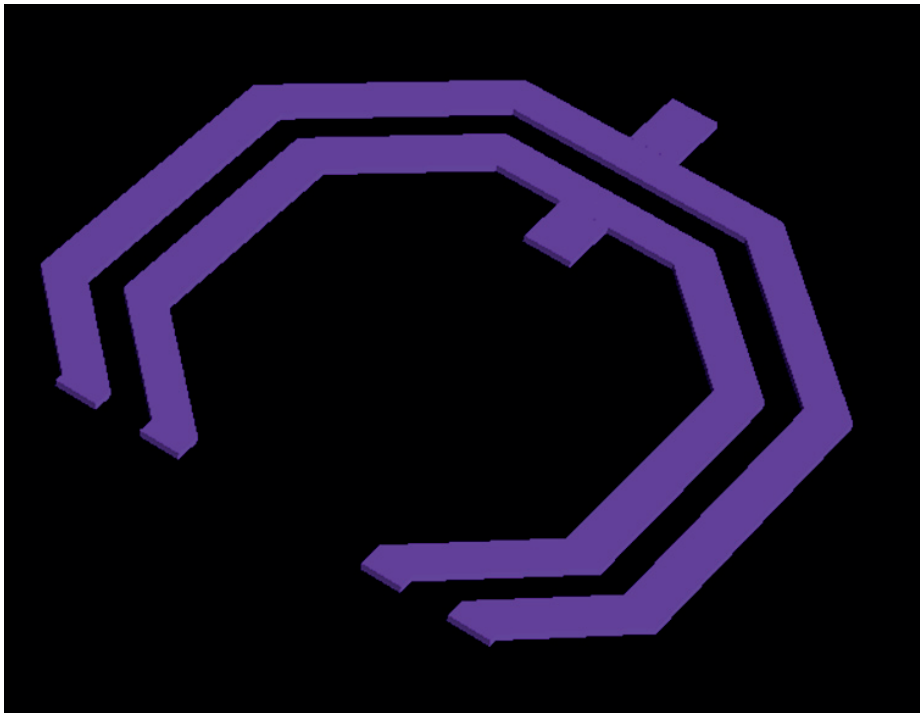


Figure 4.6: Designed Transformer for G-Band Divide-by-2 ILFD

S.No	Parameters	Values
1	Lp	112p
2	Ls	81p
3	Qp	19.8
4	Qs	24.145
5	S	3.6u
6	Wp,s	6u
7	K	0.430

Table 4.3: Design Parameters for G-Band Divide-by-2 ILFD

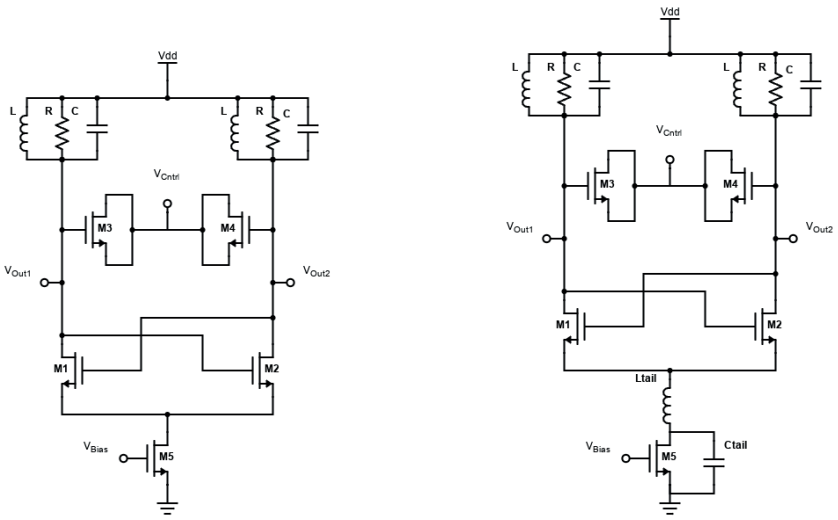
Chapter 5

mmWave VCO and ILFD

This chapter describes the design and implementation of a V-band and W-band voltage-controlled oscillator (VCO) together with a divide-by-2 injection-locked frequency divider (ILFD). It is to be noted that during this stage of design process ADS was not available so we could not design and test our own inductors, so PDK inductors were used.

5.1 V-Band

5.1.1 Tail-Filtered LC-VCO



(a) Standard LC-VCO **(b)** LC-VCO with Tail filtering

Figure 5.1: Two VCOs

In the standard cross-coupled nMOS VCO, an FET current source is used as shown in Fig 5.1(a). Phase-noise performance is optimized when the resonance tank is on the limit of being current limited[25]. In this configuration, the design is susceptible to the noise generated in the current source transistor. To improve the flicker noise performance, its length is made nine times the minimum channel length of the process. Ideally, the current source should also have high impedance at $2.f_0$ to prevent the triode resistance of the cross-coupled pairs from loading the resonator in the switched state. A source inductor is used to resonate the parasitics of the source node at $2.f_0$ as shown in the figure 5.1(b) [16]. A capacitor in parallel with the FET current source shunts high frequency noise from the current source to ground.

Two VCOs have same design values shown in Table 5.1 except tail inductor and capacitor. All widths and lengths are given in meters, capacitance given in Farads and inductance given in Henry. Sizing of capacitors and inductors are also presented for the inductor the 'w' indicates trace width, 'd' is the inner diameter and 'm' indicates number of multiples.

SNo	Parameters	Values
1	M1,2	W=16u; L = 180n
2	M3,4	W=64u; L=60n
3	M5	W=62u;L=540n;m=5
4	Tank L	L=132p;W=5um;d=61.12u
5	C Tail	C=0.42p
6	L Tail	L=80p;W=5um;d=40u

Table 5.1: Design Parameters 50GHz VCO

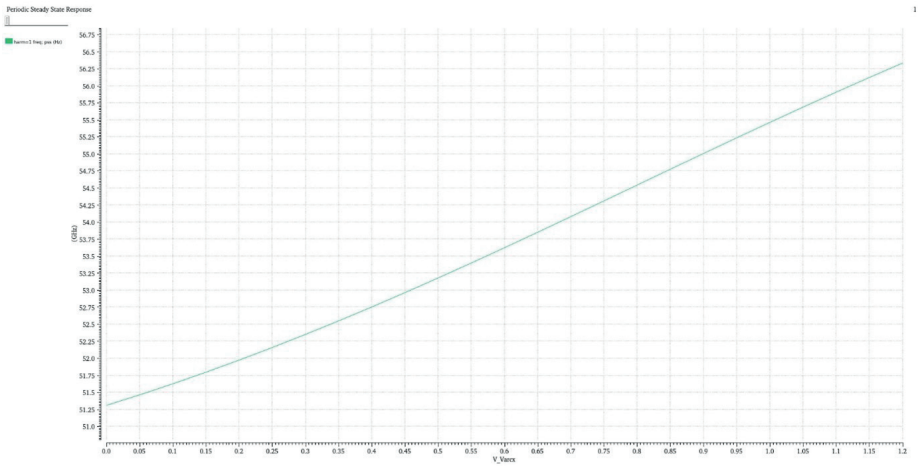


Figure 5.2: Frequency tuning characteristic for LC-VCO with Tail filtering

However, low-frequency tail current noise can still cause phase noise due to the varactor non-linearities [23]. The varactors in both the designed VCOs consist of two transistors, dimensioned to give a desired tuning range of about 10 percent as shown in Fig 5.5. The minimum channel length is used in order to maximize the varactor Q. The cross-coupled pairs are sized to provide a loop gain of 4 to fulfill the oscillation criteria[26],[22].

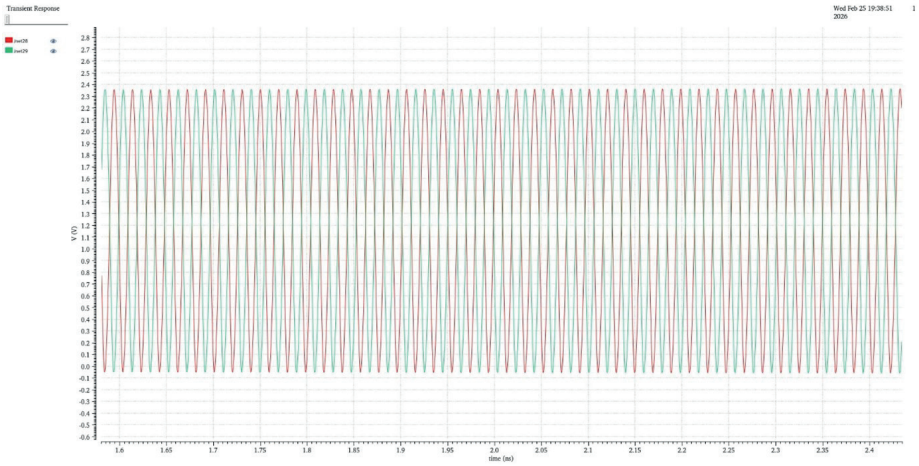


Figure 5.3: VCO Output Waveform

The VCO maintains a constant peak-to-peak output swing even when driving the ILFD load as shown in Fig 5.3.

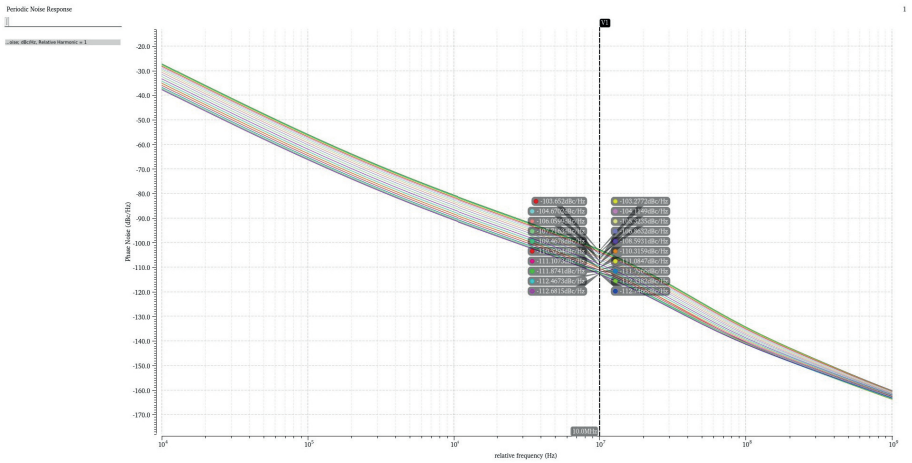


Figure 5.4: Phase noise of 50GHz VCO

The Phase noise improvement in tail filtered VCO is 4-8dB @ 1MHz offset from carrier compared

to VCO with no tail filtering as shown in Fig 5.4.

The oscillator operates at 51.1 GHz with a tuning range of 51.1−56.44 GHz (≈ 10%), achieves a phase noise of −112.75 dBc/Hz at 10 MHz offset while consuming 3.6 mW, resulting in a FoM of −181.4 dBc/Hz and a tuning-aware FoM (FoM_T) of −181.4 dBc/Hz.

5.1.2 Divide-by-2 ILFD

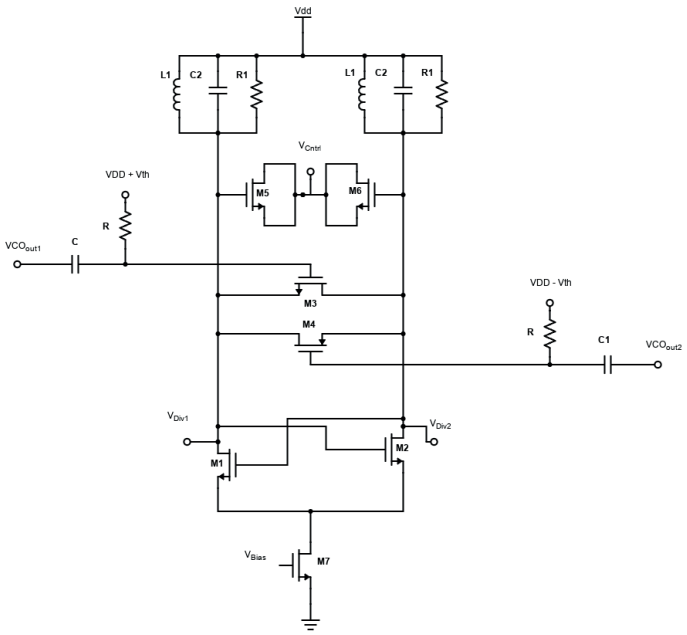


Figure 5.5: Divide-by-2 ILFD

The injection transistors were dimensioned by considering the trade-off between locking range and power consumption in direct-injection ILFDs as shwon in Fig 5.5. There exists an optimal device size where the transistors are large enough to provide sufficient injection current, while remaining small enough to avoid significantly loading the resonator tank used and increasing power consumption [13],[27].

All widths and lengths are given in meters, capacitance given in Farads and inductance given in Henry. Sizing of capacitors and inductors are also presented for the inductor the 'w' indicates turn width, 'd' is the inner diameter.

SNo	Parameters	Values
1	M1,2	W=12u; L = 120n
2	M3,4	W=64u; L=60n
3	M5,6	W=8u;L=60n
4	Tank L	L=160p;W=5um;d=72.340u
5	M7	W=42u;L=180n;m=5

Table 5.2: Design Parameters for 50GHz Divide-by-2 ILFD

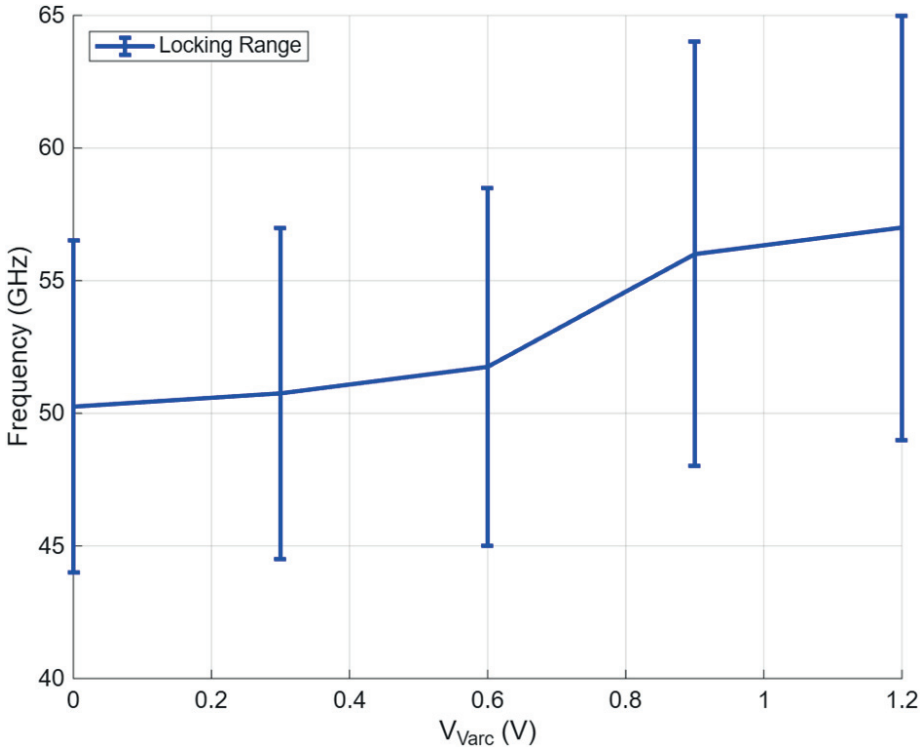


Figure 5.6: Locking range of the stand-alone ILFD vs. varactor voltage @ -1.5 dBm input power

To maximize the frequency locking range as shown in Fig 5.6, a varactor is employed for fine

frequency tuning as shown in Fig 5.7. The varactor is driven by the same control voltage as the VCO, which is generated by the loop filter in a PLL environment.

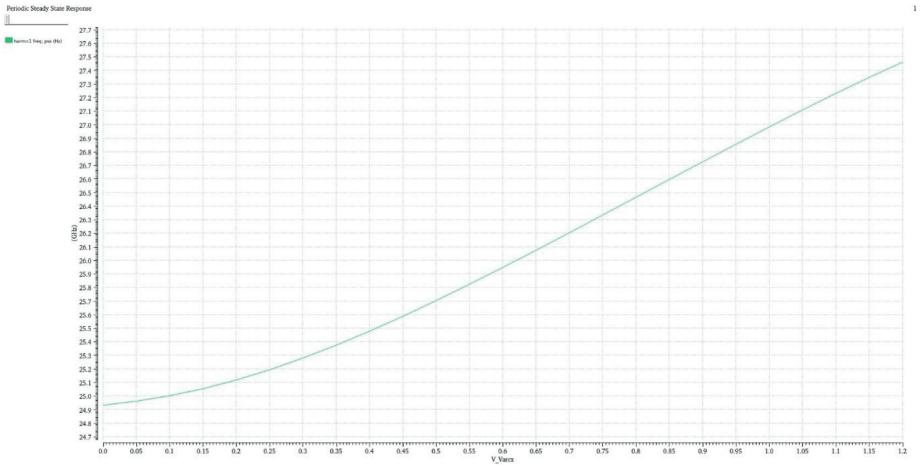


Figure 5.7: Tuning range of ILFD under the absence of injection

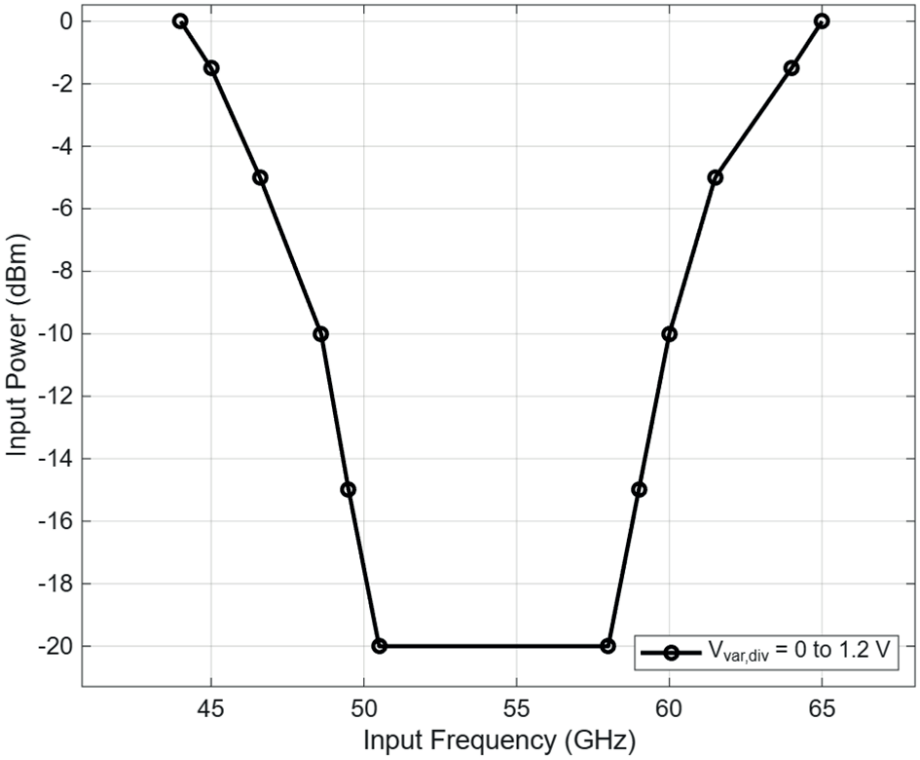


Figure 5.8: Sensitivity of the divider, using the full divider varactor voltage range @ -1.5dbm input power

It has a locking range of 20GHz from 45GHz to 65GHz at an input power of -1.5dBm for entire tuning range setting which is 36.4% relative bandwidth as shown in Fig 5.8. For a fixed tuning setting at 0.6V at -1.5dBm input power it has 11.5GHz locking range from 46GHz to 57.5GHz which is 22.23% relative bandwidth.

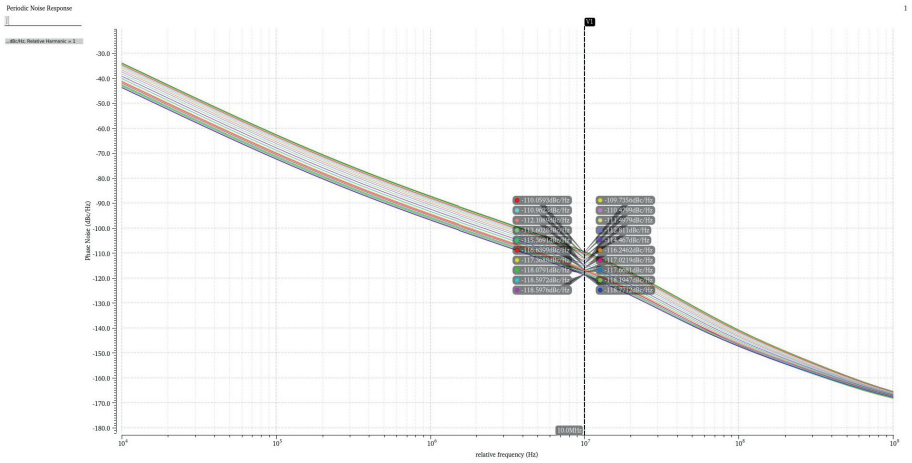


Figure 5.9: Phase noise at the output of ILFD when injected by VCO

The phase noise of at the output of ILFD when injected differential by VCO is shown in the above Fig 5.9.

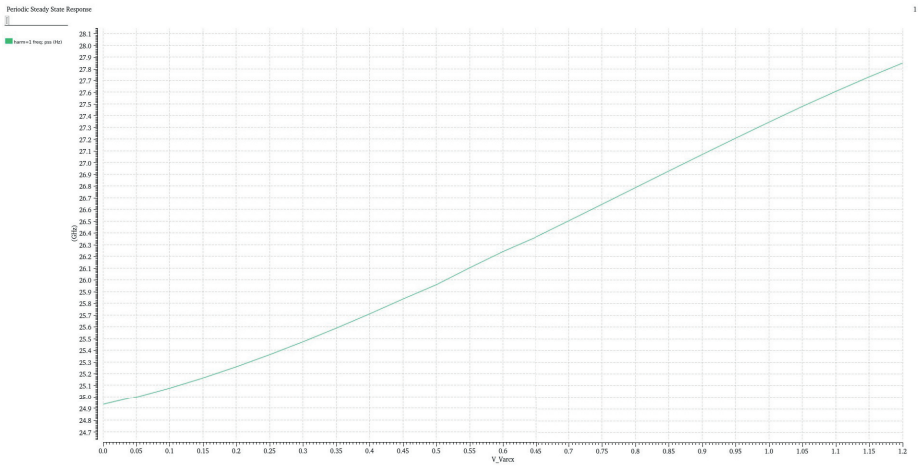


Figure 5.10: Combined tuning range of VCO and ILFD

The combined tuning range of VCO and ILFD is shown in the above Fig 5.10 The power

consumption of ILFD is 3.6mW; commbined with VCO it is 7.2mW

5.2 W-Band

5.2.1 LC-VCO

A standard LC-VCO is employed in this design without tail filtering as shown in Fig 5.11, since implementing a tail resonator becomes impractical at higher operating frequencies.

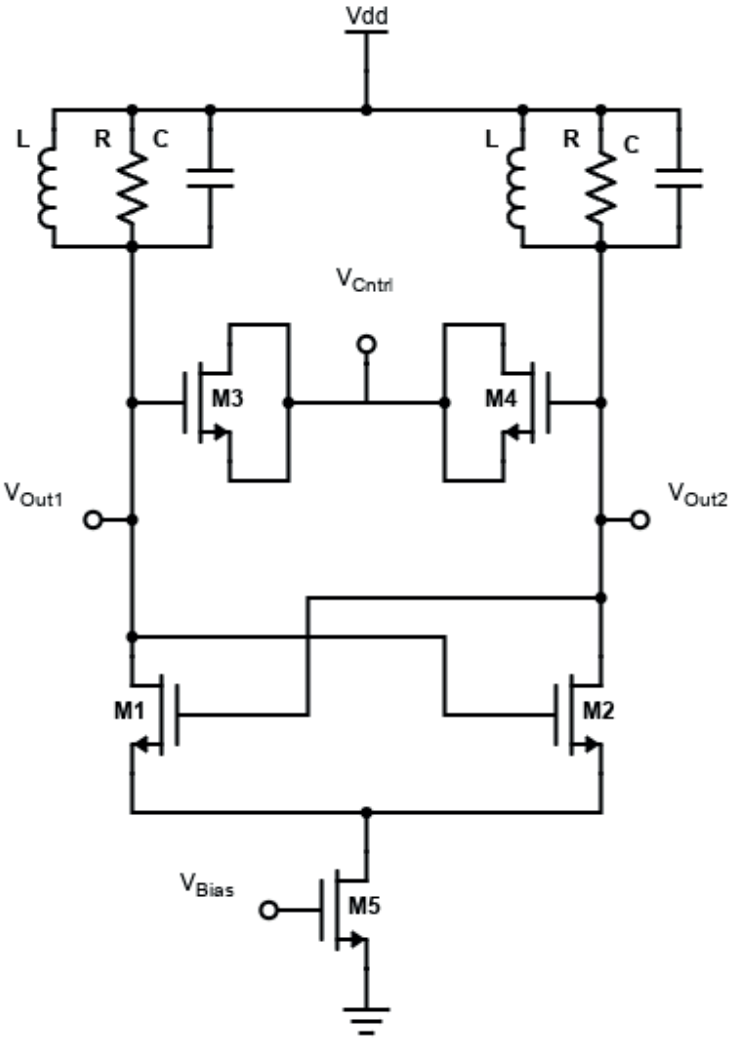


Figure 5.11: Standard LC-VCO

All widths and lengths are given in meters, capacitance given in Farads and inductance given in Henry. Sizing of capacitors and inductors are also presented for the inductor the 'w' indicates turn width, 'd' is the inner diameter as shwon in Table 5.3.

SNo	Parameters	Values
1	M1,2	W=14u; L = 60n
2	M3,4	W=38u; L=60n
3	M5	W=80u;L=180n;m=5
4	Tank L	L=76.7p;W=6um;d=37.1u

Table 5.3: Design Parameters for 90GHz VCO

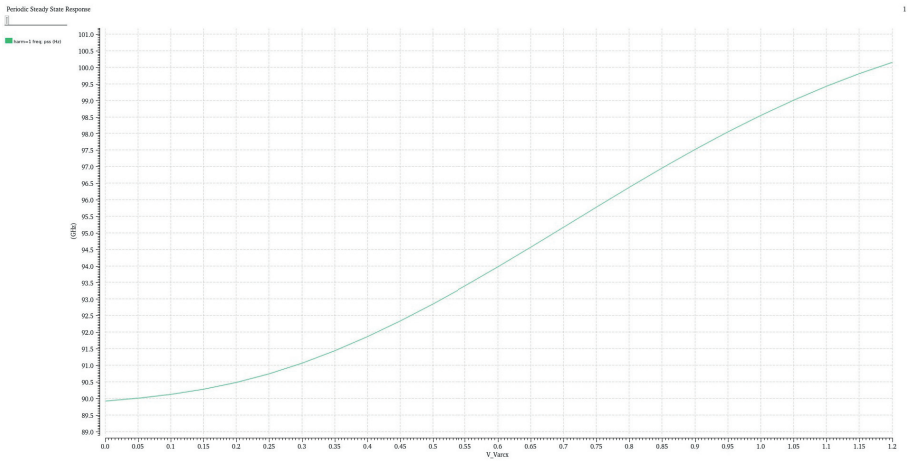


Figure 5.12: Tuning range of LC-VCO

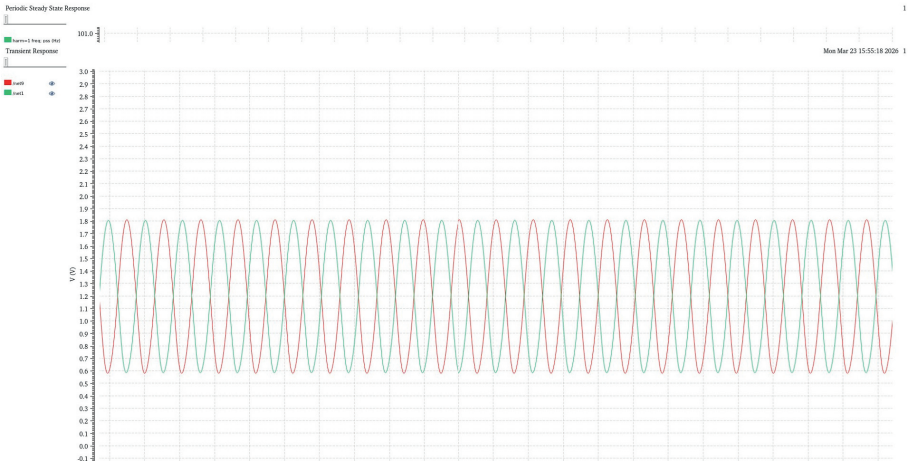


Figure 5.13: Output Waveform of VCO

The VCO maintains a constant peak-to-peak output voltage swing of 1.2V even when driving the ILFD load as shown in Fig 5.13. The cross-coupled pairs are sized to provide a loop gain of 12 to fulfill the oscillation criteria.

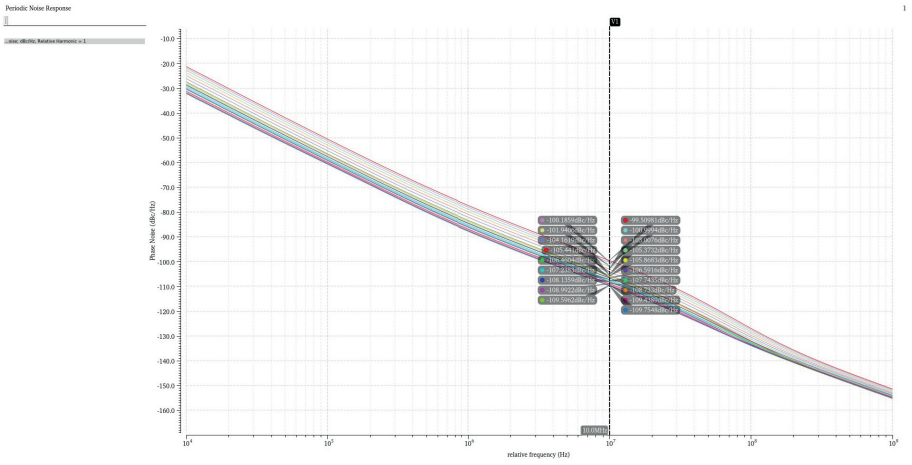


Figure 5.14: Phase Noise of VCO

The oscillator operates at $f_0 = 89.98$ GHz when $V_{\text{Varactor}} = 0$ V. The tuning range extends

from 89.98 GHz to 100.03 GHz as shown in Fig 5.12, corresponding to a total tuning range of 10.05 GHz. The best simulated phase noise is -109.4 dBc/Hz at a 10 MHz offset frequency when the varactor control voltage is 0 V as shown in Fig 5.14. The DC power consumption of the oscillator is 3.2 mA $\times$ 1.2 V, resulting in 3.84 mW. Based on these parameters, the calculated figure-of-merit (FoM) is approximately -182.6 dBc/Hz, while the tuning-range-enhanced figure-of-merit (FoMT) is approximately -183.6 dBc/Hz.

5.2.2 Divide-by-2 ILFD

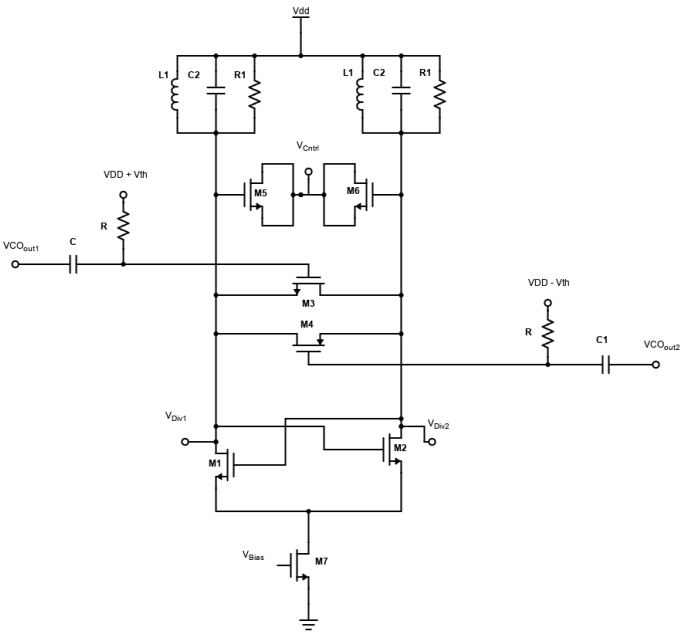


Figure 5.15: Divide-by-2 ILFD

The Schematic of ILFD is shown in Fig 5.15. All widths and lengths are given in meters, capacitance given in Farads and inductance given in Henry. Sizing of capacitors and inductors are also presented for the inductor the 'w' indicates turn width, 'd' is the inner diameter.

SNo	Parameters	Values
1	M1,2	W=12u; L = 120n
2	M3,4	W=64u; L=60n
3	M5	W=42u;L=180n;m=5
4	M6,7	W=8u;L=60n
5	Tank L	L=175p;W=5um;d=78.260u

Table 5.4: Design Parameters for 90GHz Divide-by-2 ILFD

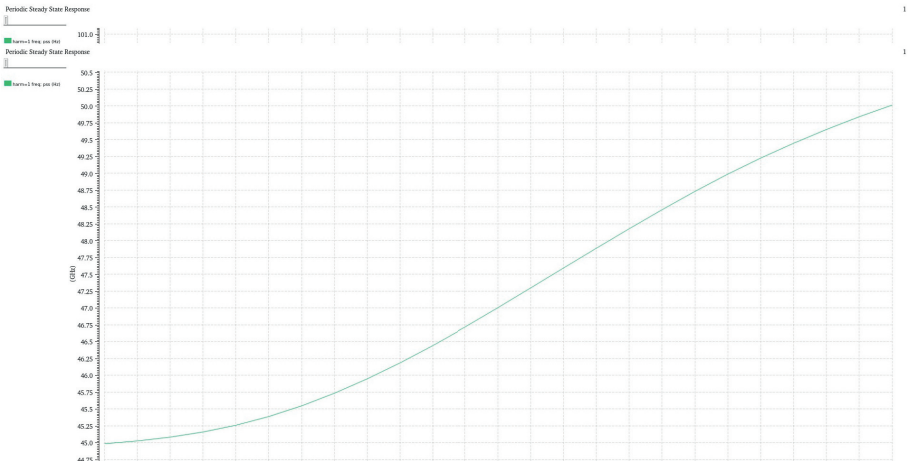


Figure 5.16: Tuning range of ILFD; under absence of injection

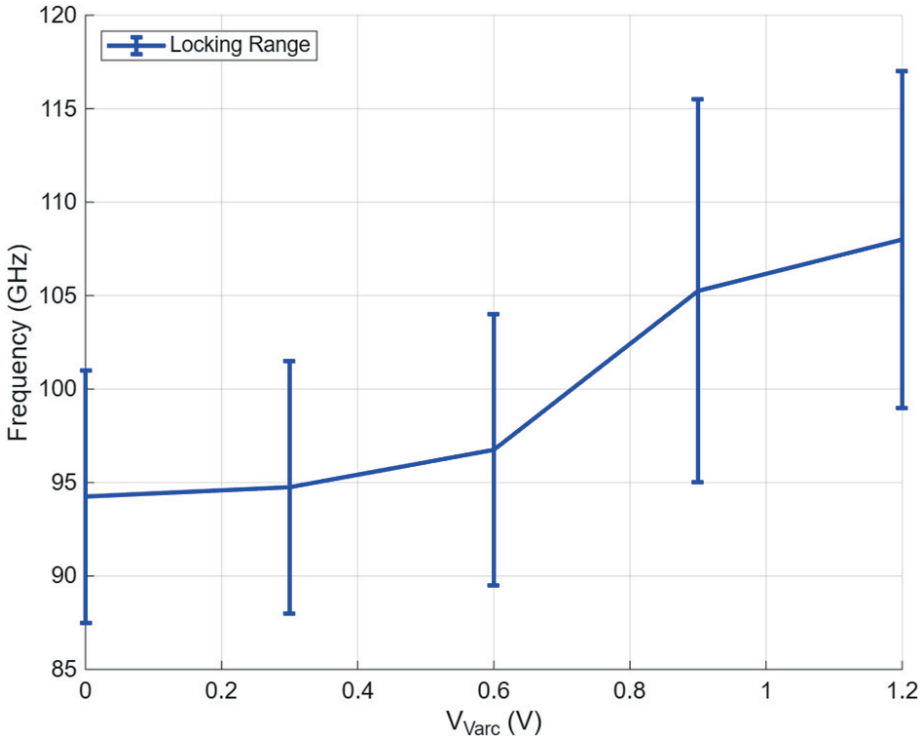


Figure 5.17: Locking range of the stand-alone ILFD vs. varactor voltage

The tuning tange of ILFD is shown in Fig 5.16 To maximize the frequency locking range, a varactor is employed for fine frequency tuning as shown in Fig 5.17. The varactor is driven by the same control voltage as the VCO, which is generated by the loop filter in a PLL environment.

It has a locking range of 29.5GHz from 87.5GHz to 117GHz at a input power of -1.5dBm for entire tuning range setting which is 28.85% relative bandwidth.For a fixed tuning setting at 0.6V at -1.5dBm input power it has 14.5GHz locking range from 89.5GHz to 104GHz which is almost 15% relative bandwidth.

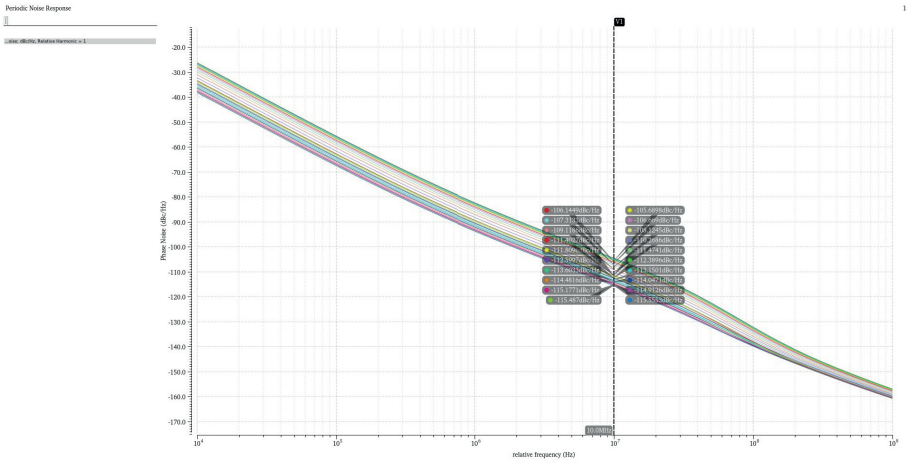


Figure 5.18: Phase noise at the output of ILFD when injected by VCO

The phase noise of at the output of ILFD when injected differential by VCO is shown in the above Fig 5.18.

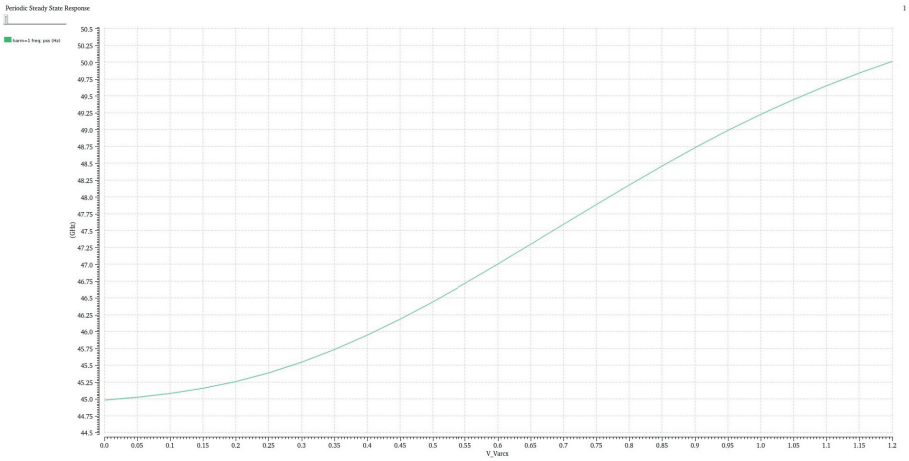


Figure 5.19: Combined tuning range of VCO and ILFD

The combined tuning range of VCO and ILFD is shown in the above Fig 5.19. The power

consumption of ILFD is 3.6mW; combined with VCO it is 7.44mW

Chapter 6

Designed Sub-terahertz VCO and ILFDs

In this chapter the designed sub-terhertz VCO and Divide-by-2 ILFDs are presented; all are tuned using magnectic tuning. The inductors designed and discussed in the previous section are utilized in the implementation of the proposed circuits.

6.1 Magnetically Tuned VCO

The biasing is implemented using a PMOS transistor to improve noise performance as shown in Fig 6.1. PMOS devices generally exhibit lower flicker noise than NMOS transistors due to reduced carrier mobility and fewer interface trapping effects.

NMOS transistors are used in the cross-coupled pair. Although improved phase noise performance can be achieved by using PMOS transistors instead of NMOS, the lower carrier mobility of PMOS devices requires significantly larger transistor widths to provide the same transconductance and startup gain needed to sustain oscillation. The increased device size introduces additional parasitic capacitance, which reduces the maximum oscillation frequency achievable. Therefore, NMOS devices are preferred in this design to enable operation at higher frequencies

For phase noise optimization, the channel length of the cross-coupled transistors in a VCO is often chosen to be larger than the minimum length to reduce the transistor noise. However, the noise summary analysis performed in this design showed that improved phase noise performance was achieved with shorter channel lengths. Therefore, a minimum channel length of 60 nm was used for cross-coupled transistors. The cross-coupled pairs are sized to provide a loop gain of 14 to fulfill the oscillation criteria.

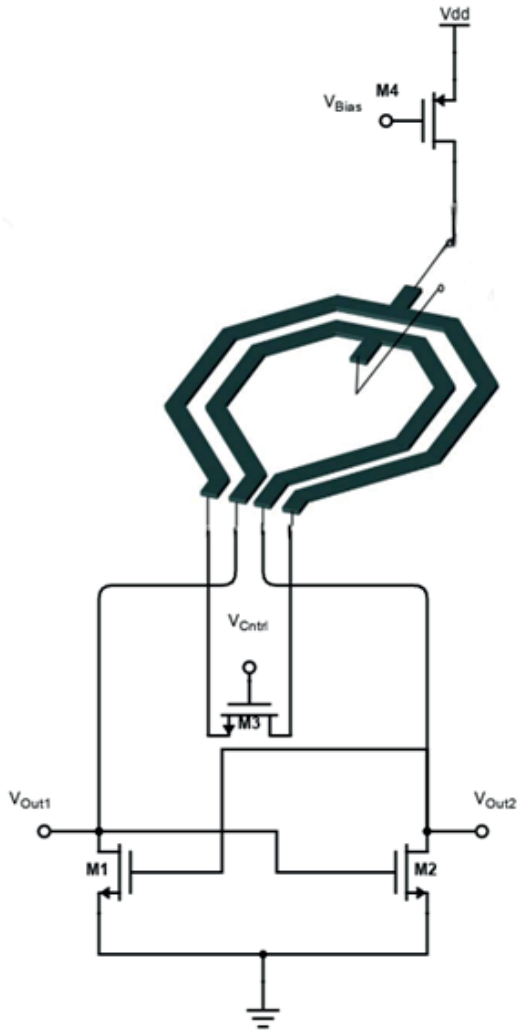


Figure 6.1: Magnetically Tuned VCO

SNo	Parameters	Values
1	M1,2	W = 12u; L = 60nm
2	M3	W = 48u; L = 280nm;m = 5
3	M4	W = 8u; L = 60nm

Table 6.1: Design Parameters for D-Band VCO

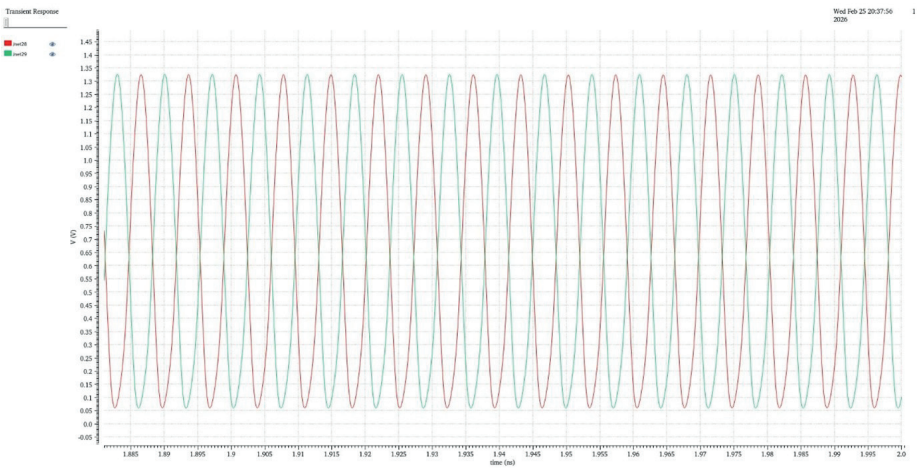


Figure 6.2: Output Waveform

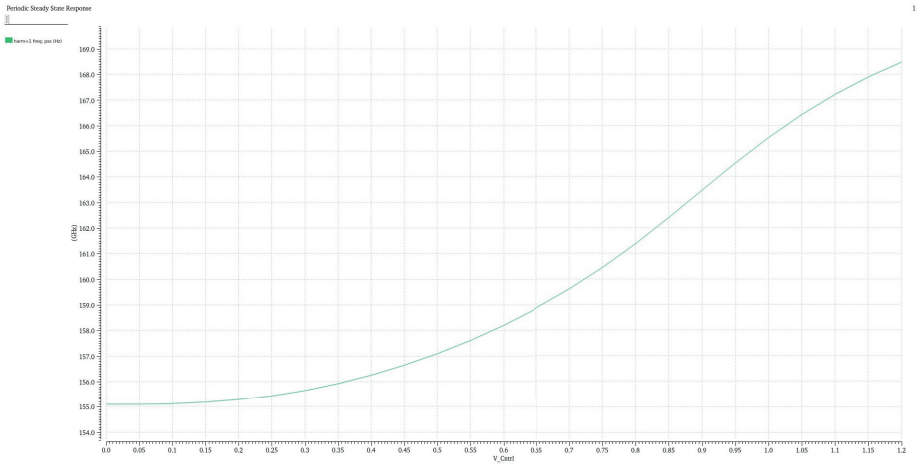


Figure 6.3: Unloaded Tuning Range of VCO

The VCO was biased to a DC current of 3mA, with a power consumption of 3.6mW. The VCO output is fed differentially to an injection-locked frequency divide-by-2. Simulations show that when using the differential output of the VCO as shown in Fig 6.2, the input signal to the ILFD is strong enough to make its lock range cover the VCO tuning range without changing its tuning setting. The stand alone tuning range of the VCO is shown in Fig 6.3.

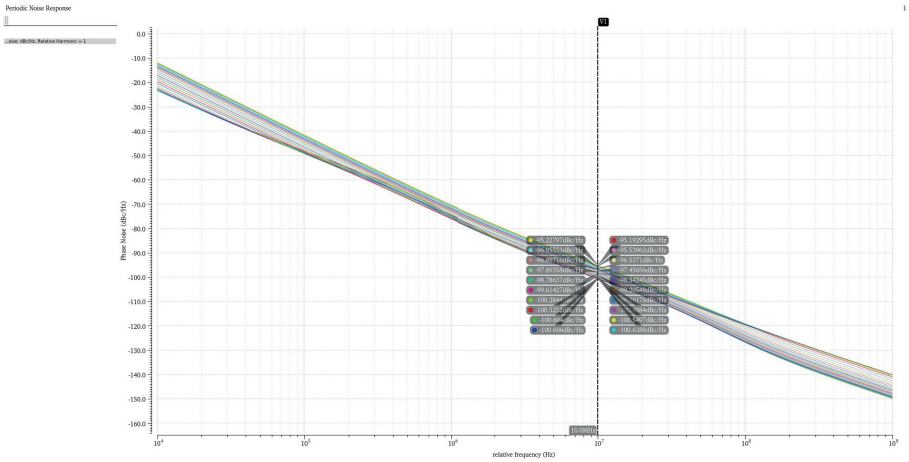


Figure 6.4: Phase Noise of VCO for all tuning settings

The stand alone phase noise of the VCO is shown in Fig 6.4. The oscillator achieves a FoM of $-179\,\mathrm{dBc/Hz}$ and a tuning-aware FoM ($\mathrm{FoM_T}$) of $-177.7\,\mathrm{dBc/Hz}$.

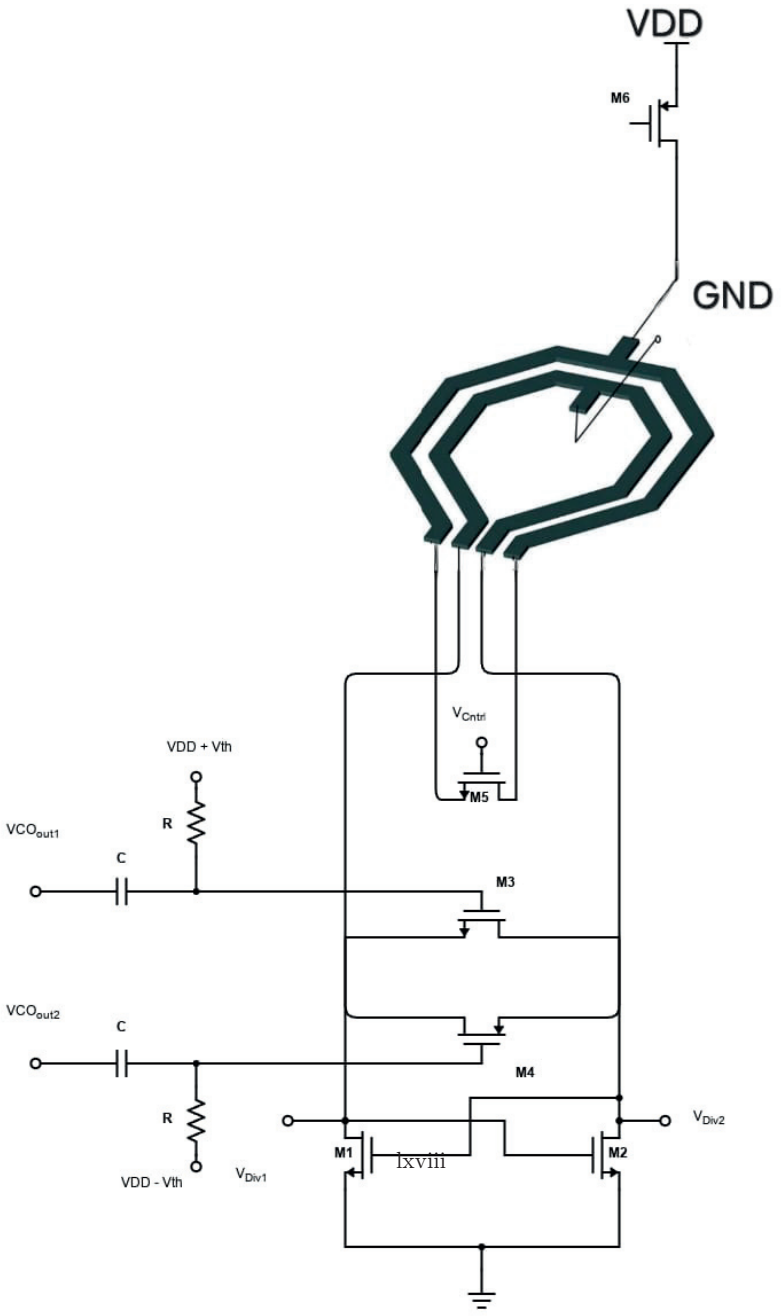


Figure 6.5: Divide-by-2 ILFD

The schematic of ILFD is shown in Fig 6.5 The phase noise floor of an injection-locked frequency divider (ILFD) is typically of limited concern at mm-wave frequencies. However, at sub-terahertz frequencies, the phase noise of the ILFD becomes more significant, as the injection devices introduce additional noise that can degrade the overall phase noise performance. To mitigate this effect, a PMOS current source was employed to improve the noise performance, as explained in the previous section.

SNo	Parameters	Values
1	M1,2	W = 22u; L = 60nm
2	M3,4	W = 48u; L = 180nm ;m = 5
3	M5	W = 8u; L = 120nm
4	M6	W = 8u; L = 120nm

Table 6.2: Design Parameters for D-Band Divide-by-2 ILFD

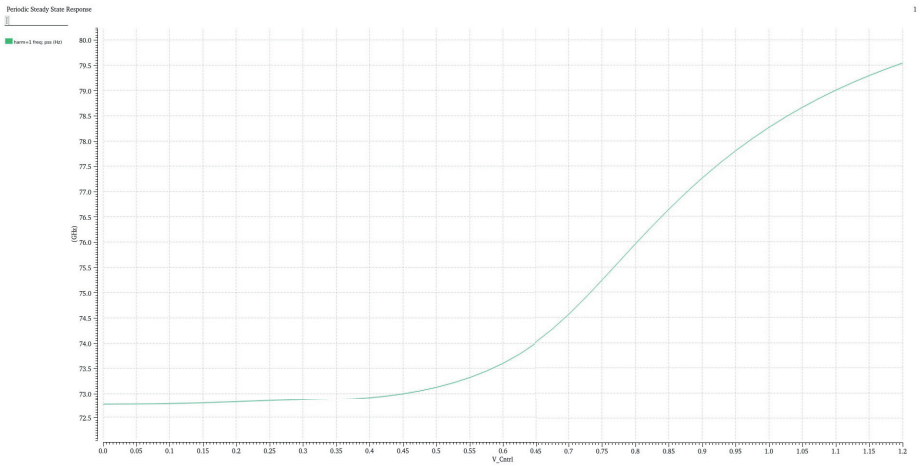


Figure 6.6: Tuning range from 0 to 1.2V

Typically, injection transistors are sized with the minimum channel length to maximize conversion gain or injection efficiency. However, simulations of this design revealed an issue that the tuning range stagnates from 0 V to 0.49 V, corresponding to the threshold voltage of the magnetic tuner switch, as shown in the Fig 6.6. To address this, the channel length was increased to twice the minimum, which raises the transistor's output resistance. This reduces loading on the resonator, preserving its Q factor and improving the tuning linearity. The resulting enhancement is illustrated

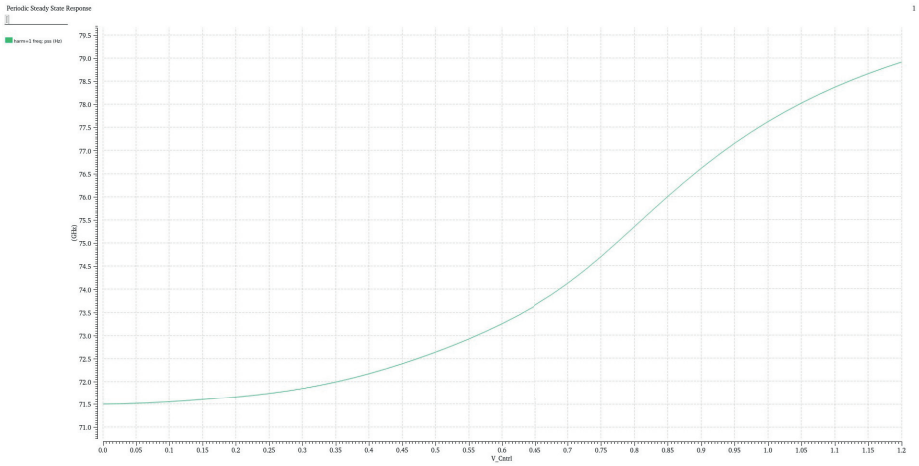


Figure 6.7: Improved Tuning range from 0 to 1.2V

in Fig 6.7.

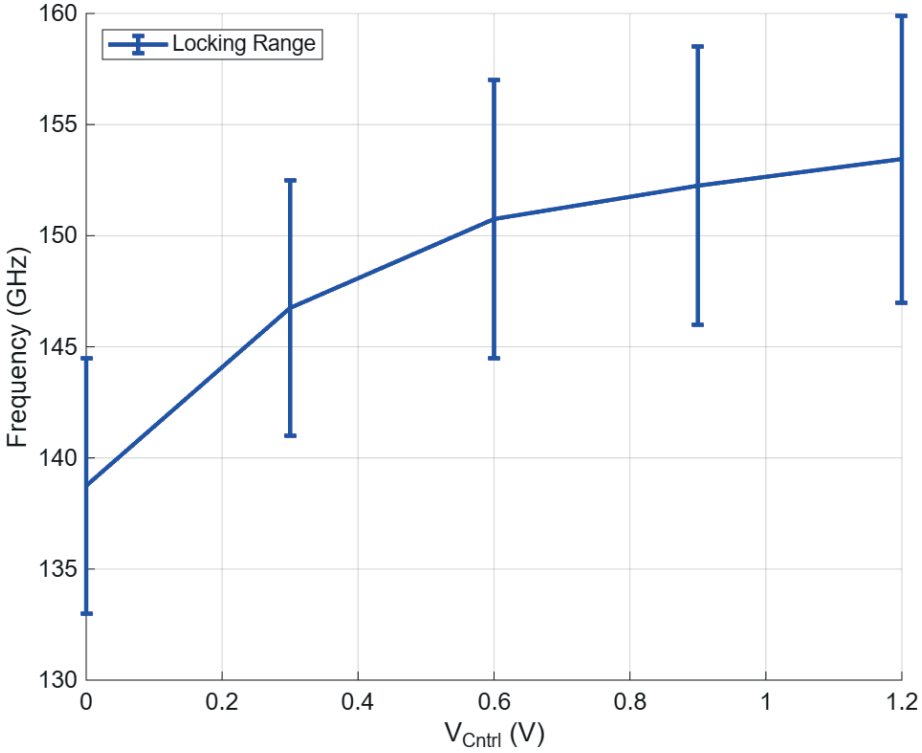


Figure 6.8: Tuning range from 0 to 1.2V

To maximize the frequency locking range, magnetic tuning is employed for fine frequency tuning as shown in Fig 6.8. The ILFD is driven by the same control voltage as the VCO, which is generated by the loop filter in a PLL environment.

[H]

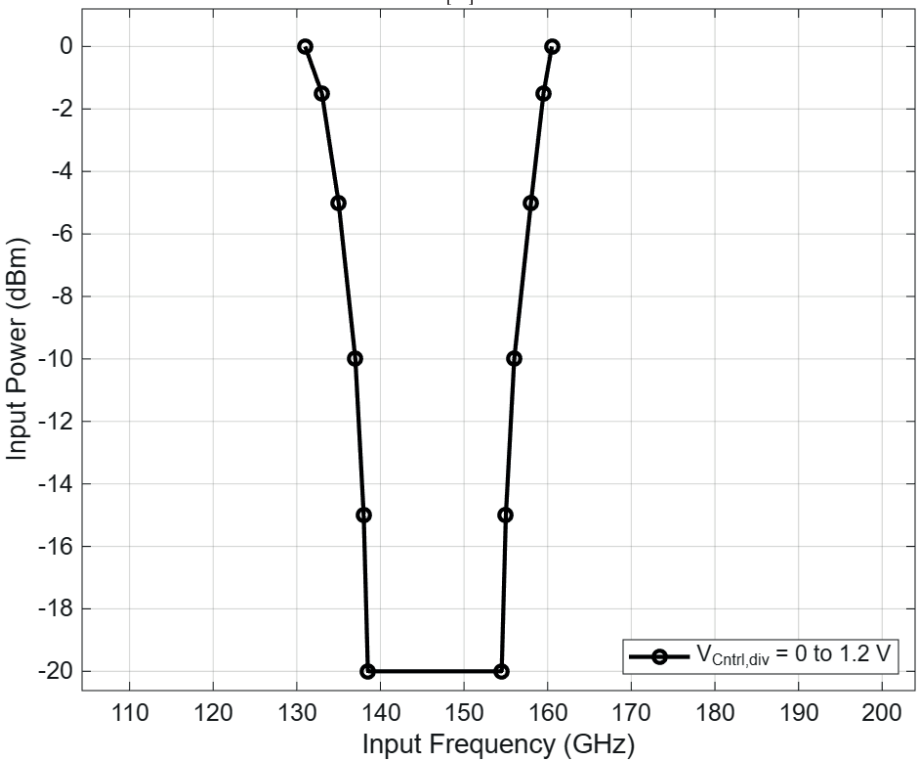


Figure 6.9: Locking range from 0 to 1.2V

It has a locking range of 26.5GHz from 133GHz to 159.5GHz at a input power of -1.5dBm for entire tuning range setting which is 18.12% relative bandwidth as shown in Fig 6.9. For a fixed tuning setting at 0.6V at -1.5dBm input power it has 12.5GHz locking range from 144.5GHz to 157GHz which is 8.3% relative bandwidth.

6.3 Combined VCO and ILFD

Due to the complexity of designing a wideband buffer stage at sub-terahertz frequencies and the limited achievable bandwidth for effective isolation, the VCO and ILFD are directly connected through a AC coupling capacitor. As the VCO directly drives the ILFD, the parasitic capacitances introduced by the ILFD load the VCO tank, resulting in a reduction in the oscillation frequency compared to the unloaded VCO.

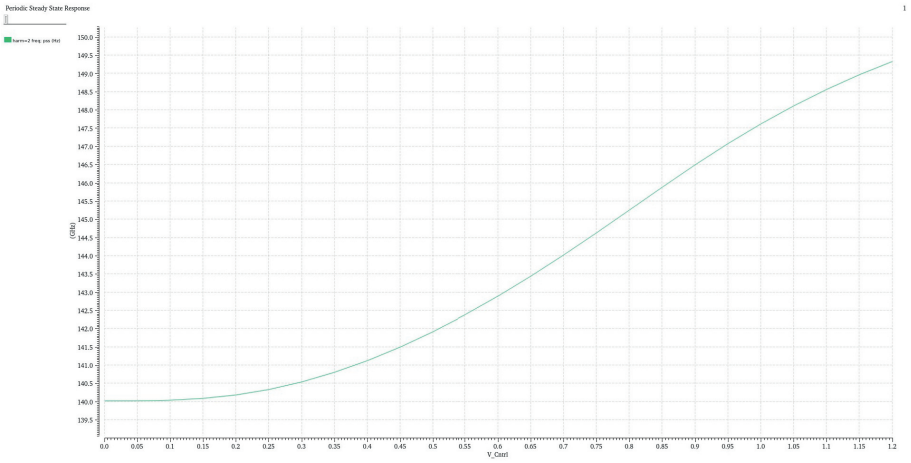


Figure 6.10: Tuning Range of VCO When driving ILFD

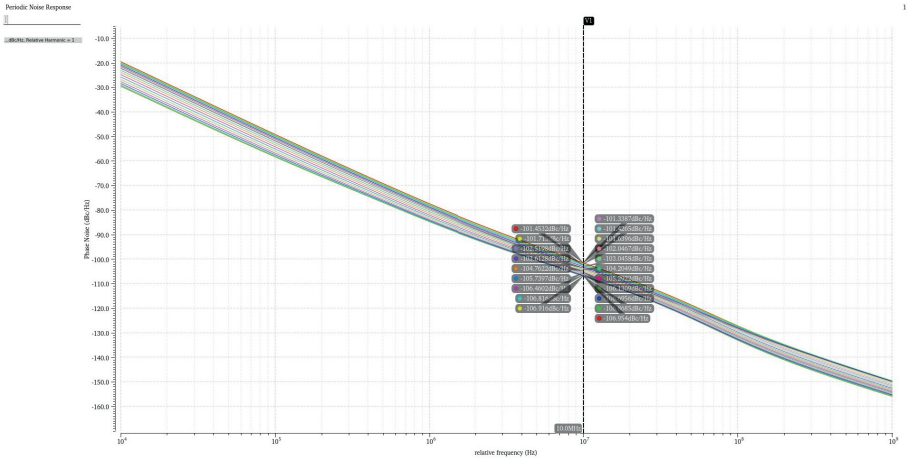


Figure 6.11: Phase noise of the combined VCO and ILFD

The new oscillation frequency when driving the ILFD is $f_0 = 140$ GHz with a tuning range of $\Delta f_{\text{tuning}} = 9.3$ GHz as shown in Fig 6.10. The DC power consumption of the oscillator is $P_{\text{DC}} = 3.6$ mW, and the simulated phase noise at a 10 MHz offset is $L(\Delta f) = -100.64$ dBc/Hz as shown in Fig 6.11. Using these parameters, the figure-of-merit (FoM) is -178 dBc/Hz, and

the tuning-range-enhanced figure-of-merit (FoMT) is −174.2 dBc/Hz. These results show that the VCO maintains comparable phase noise performance while operating at a higher frequency with a tuning range of 6.43% and moderate power consumption.

The total power consumption of VCO and ILFD is 7.2mW

6.4 A Magnetically Tuned 200GHz divide by 2 ILFD

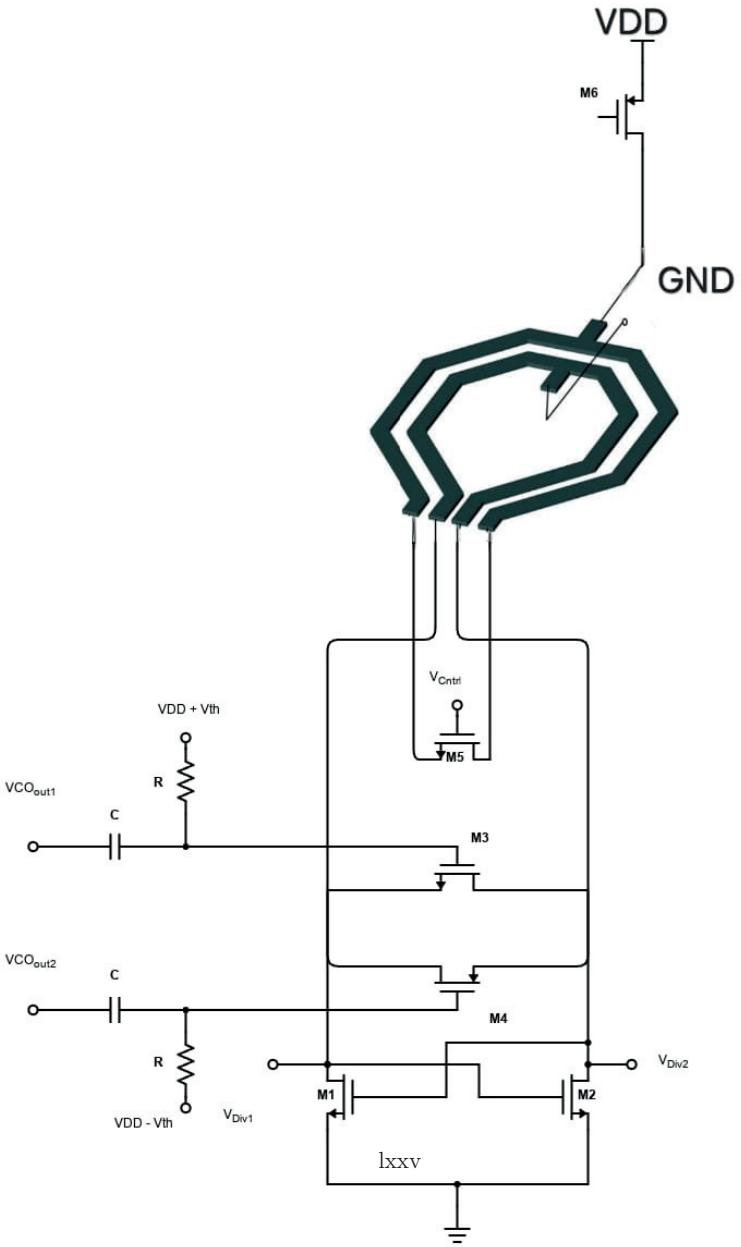


Figure 6.12: 200GHz divide-by-2 ILFD

SNo	Parameters	Values
1	M1,2	W = 12u; L = 60nm
2	M3,4	W = 6u; L = 120nm
3	M5	W = 8u ; L = 60nm
4	M6	W = 36u ; L = 180nm

Table 6.3: Design Parameters for G-Band Divide-by-2 ILFD

The schematic of ILFD is shown in Fig 6.12 A similar issue was observed while simulating the tuning range, where the tuning range remained stagnant from 0 V to approximately 0.49 V, corresponding to the threshold voltage of the magnetic tuner switch as shown in Fig 6.13. To mitigate this effect, the channel length of the transistor was increased to twice the minimum value. However, this modification resulted in only a slight improvement. Therefore, the threshold voltages bias (V_{th}) of the NMOS and PMOS injection transistors were reduced. A higher bias voltage keeps the injection transistors more strongly turned on, enabling stronger mixing and improved injection locking. However, excessive conduction may also drain energy from the oscillator and degrade the oscillation amplitude. Lowering the threshold voltages bias allows the injection transistors to operate effectively across the entire tuning range. Vth bias of NMOS was reduced from 546.1 mV to 515mV and the Vth bias of PMOS was reduced from 480mV to 470mV as shown in Fig 6.14

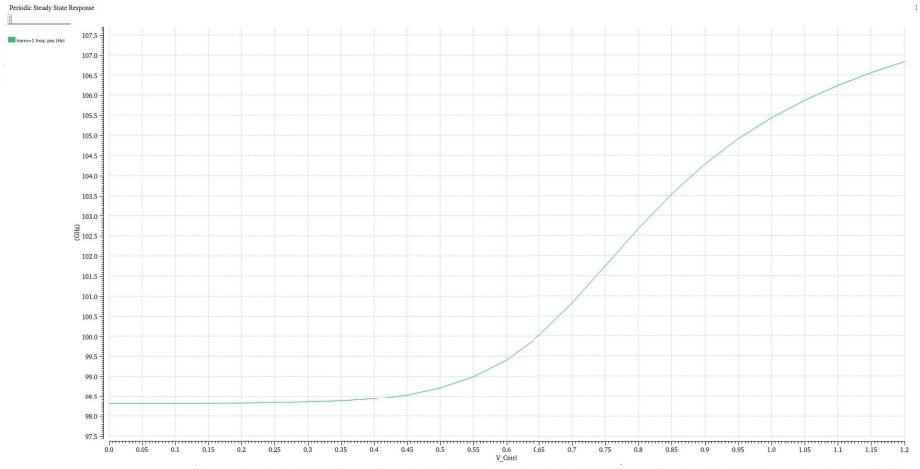


Figure 6.13: TR of 200GHz ILFD

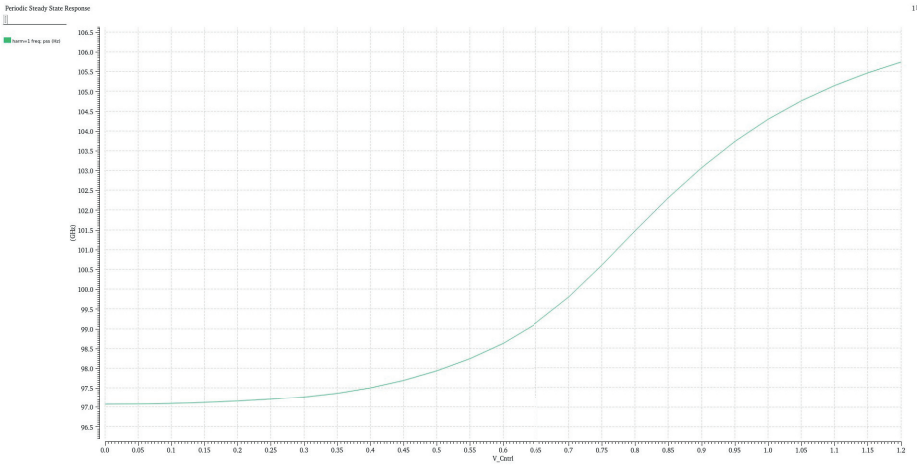


Figure 6.14: Improved TR of 200GHz ILFD

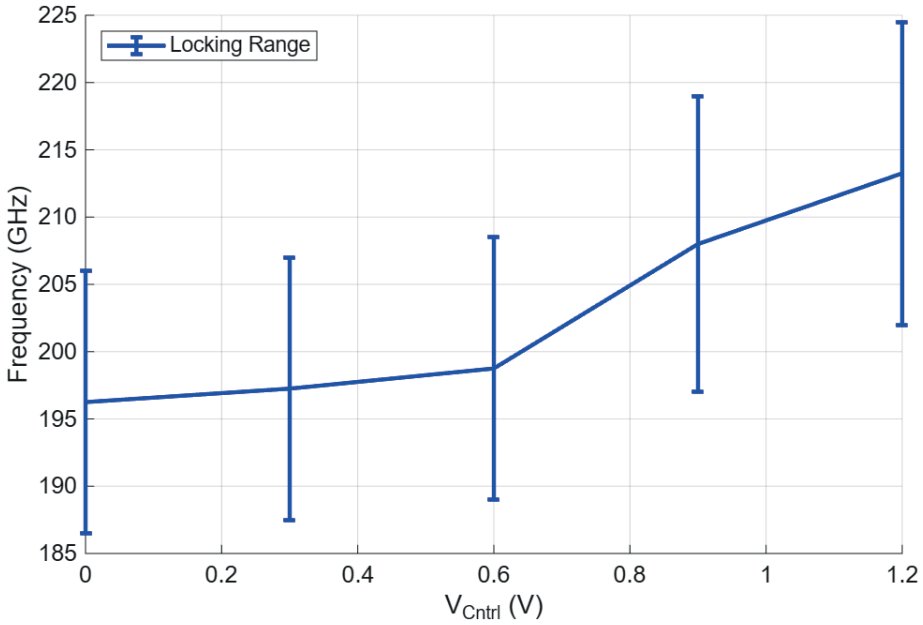


Figure 6.15: Tuning range from 0 to 1.2 V @ -1.5 dBm input power

To maximize the frequency locking range, a magnetic tuning is employed for fine frequency tuning as shown in Fig. The ILFD is driven by the same control voltage as the VCO, which is generated by the loop filter in a PLL environment.

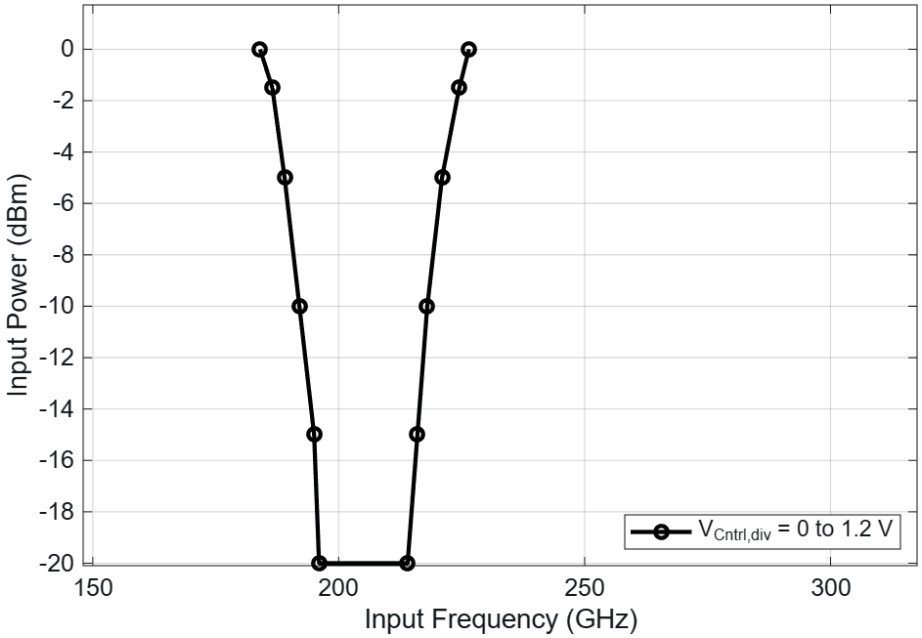


Figure 6.16: Locking range from 0 to 1.2 V @ -1.5 dBm input power

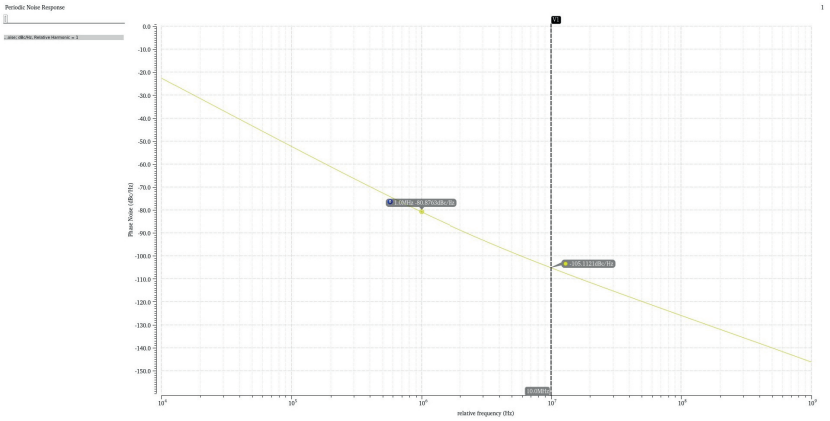


Figure 6.17: Phase noise of ILFD under no injection

It has a locking range of 38GHz from 186.5GHz to 224.5GHz at a input power of -1.5dBm for entire tuning range setting as shown in Fig 6.1 which is 19.34% relative bandwidth.For a fixed tuning setting at 0.6V at -1.5dBm input power it has 19.5GHz locking range from 189GHz to 208.5GHz which is 9.874% relative bandwidth.The noise floor of the ILFD is -105.1 dBc/Hz at 10 MHz as shown in Fig 6.17. The power conumption is 4.2mW

Chapter 7

Conclusions and Future work

Table 7.1: Summary and Comparison of D-Band Fundamental VCOs

Ref	Freq (GHz)	TR (%)	V_{DD} (V)	Power (mW)	Phase Noise (dBc/Hz)	FoM (dBc/Hz)	FoMT (dBc/Hz)	P_{out} (dBm)	DC-RF (%)	Process
[28]	175.6	0.34	1.65	25.8	-101.7@1 MHz	-195.4	-166.1	4.8	11.7	130 nm SiGe
[29]	161.1	4.7	4.6	46.5	-85.2@1 MHz	-172.7	-161.1	-15	0.07	250 nm SiGe
[24]	162.1	5.2	0.7	5.6	-105@10 MHz	-181	-176.2	-9.3	2.1	65 nm CMOS
[30]	118	7.8	1	5.6	-83.9@1 MHz	-181.8	-175.5	–	–	65 nm CMOS
[31]	125	3.4	1	17	-99.3@1 MHz	-188.9	–	–	–	65 nm CMOS
[32]	128.76	0.62	1.4	11.2	-82@1 MHz	–	–	-10.6	–	65 nm CMOS
This Work	139.8	6.37	1.2	3.6	-100.855@10 MHz	-178	-174.2	–	–	65 nm CMOS

Table 7.2: Summary and Comparison of D-Band Fundamental VCO

The performance of the proposed VCO is compared with previously reported millimeter-wave oscillators in Table 7.1. The proposed design operates at 140 GHz with a tuning range of 6.43%, which is comparable to or larger than several prior works, such as [28] and [32], and close to designs such as [9]. Despite operating at a high frequency, the proposed VCO achieves a relatively low DC power consumption of only 3.6 mW from a 1.2 V supply, which is significantly lower than many reported oscillators, including [28], [29], [31] and [24] where no tail current source is used. The phase noise performance is -100.64 dBc/Hz at the reported offset frequency, resulting in a figure-of-merit (FoM) of -178 dBc/Hz and a tuning-aware figure-of-merit (FoMT) of -174.2 dBc/Hz. The output power and DC-to-RF efficiency cannot be measured in this work because it depends on the RF power delivered to a load, and no output buffer was implemented. Although some SiGe implementations achieve slightly better FoM due to the advantages of the technology node, they typically require substantially higher power consumption and supply voltage. In contrast, the proposed design implemented in 65 nm CMOS achieves a favorable trade-off between tuning range, phase noise, and power efficiency.

The performance of the proposed injection-locked frequency divider (ILFD) is compared with recent works in Table 7.2. The operating frequency range of the proposed design spans 133–154.5 GHz, which is among the widest reported for 65 nm CMOS ILFDs. It achieves a locking range (LR) of 18.12%, comparable to the highest values in the literature (e.g., 19.8% in [34]),

Table 7.3: Comparison of D-Band Frequency Dividers

Ref	Freq (GHz)	LR (%)	Input Power (dBm)	V_{DD} (V)	Power Cons. (mW)	Divide Type	Div. Ratio	Technology
[33]	124.3–139	11.2	< -2	1.1	6.27	Injection-Locked	2	65 nm CMOS
[34]	135.2–165	19.8	0	1.2	4.7	Injection-Locked	2	65 nm CMOS
[33]	153.3–162.8	6.0	< -2	1.1	6.27	Injection-Locked	2	90 nm CMOS
[35]	128.24–137	6.6	< -2	1.1	5.5	Injection-Locked	2	65 nm CMOS
[36]	132.7–143.5	7.8	< -4	1.1	5.27	Injection-Locked	2	65 nm CMOS
This Work	133–154.5	18.12	-1.5	1.2	3.6	Injection-Locked	2	65 nm CMOS

Table 7.4: Summary and Comparison of D-Band ILFD

while requiring a moderate injection power of -1.5 dBm. The supply voltage is 1.2 V, and the total DC power consumption is only 3.6 mW, which is the lowest among the compared 65 nm designs, highlighting its energy-efficient operation. All referenced works use divide-by-2 injection-locked architectures, and the proposed ILFD maintains this standard while providing enhanced LR, reduced power consumption, and wide frequency coverage.

Table 7.5: Summary and Comparison of G-Band ILFDs

Ref	Freq (GHz)	LR (%)	Input Power (dBm)	V_{DD} (V)	Power Cons. (mW)	Divide Type	Div. Ratio	Technology
[37]	181–208	13.88	0	1.0	2.4	Injection-Locked	2	65 nm CMOS
[38]	198.9–201	1.05	-15	1.1	8.8	Injection-Locked	2	65 nm CMOS
[33]	192.4–194.06	0.86	-15	1.2	22.8	Injection-Locked	2	90 nm CMOS
[39]	297.08–306.64	3.17	-5 (est.)	0.9	9.18	Injection-Locked	5	40 nm CMOS
This Work	186.5–224.5	19.34	-1.5	1.2	4.2	Injection-Locked	2	65 nm CMOS

The performance of the proposed 200 GHz injection-locked frequency divider (ILFD) is compared with recently reported designs in Table 7.3. The proposed divider operates over a frequency range of 186.5–224.5 GHz, corresponding to a locking range (LR) of 19.34%, which is significantly wider than most previously reported works. For example, designs in [38] and [33] exhibit very narrow locking ranges of 1.05% and 0.86%, respectively, while [37] achieves a moderate LR of 13.88%. Although the design in [39] operates at a higher frequency band, it only achieves a locking range of 3.17%. In terms of power consumption, the proposed ILFD dissipates 4.2 mW from a 1.2 V supply, which is considerably lower than several prior works, such as [33] (22.8 mW) and [38] (8.8 mW), while remaining competitive with low-power designs like [37].

The presented designs demonstrate the feasibility of achieving high-performance mm-wave oscillators and injection-locked frequency dividers with competitive phase noise, power consumption, and tuning range in simulation.

However, the physical layout has not yet been completed and remains an important part of the future work. Careful layout implementation will be essential to properly address gate resistance,

routing parasitics, and parasitic capacitances, all of which strongly affect performance at mm-wave and sub-terahertz frequencies. Special attention must be given to symmetric routing, shielding, and ground integrity.

Future work could explore a magnetic transformer to AC-couple the gates of the cross-coupled transistors to the LC tank [40]. The passive voltage gain provided by the transformer reduces the contribution of the active devices to the $1/f^2$ phase noise beneficial for improving overall phase-noise performance in sub-terahertz VCO designs.

Ultimately, the most important next step is to complete the layout and proceed to tapeout. Fabrication and measurement of the chip are necessary to validate the simulation results, evaluate PVT robustness, and confirm the practical feasibility of the proposed architecture in silicon.

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