A Low Power Dual-Path Sub-Sampling PLL Covering 2GHz-4GHz

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Abstract

Ring voltage-controlled oscillators (Ring VCOs) are widely used in clock generation because of their compact area and wide tuning range, but their high inherent phase noise limits their application in high-performance systems. To address this, this thesis presents a low-power dual-path sub-sampling PLL (SSPLL) covering a wide frequency range from 2GHz to 4GHz. To effectively suppress the phase noise from the Ring VCO, this design employs a sub-sampling phase detector and charge pump (SSPD/SSCP) architecture to drastically increase the bandwidth of PLL, and also reduce the in-band noise. Meanwhile, a dual-path topology is introduced to further widen the loop bandwidth. Furthermore, an Automatic Frequency Calibration (AFC) algorithm is adopted to accelerate the locking process. The proposed circuit is designed and simulated in a 65nm CMOS process. When operating at an output frequency of 2.05 GHz, the total power consumption is only 6 mW. The RMS jitter is optimized to 1.24 ps (integrated from 100KHz to 100MHz), and the phase noise reaches -111 dBc/Hz at 10 MHz offset.
Keywords: *SSPLL, VCO, AFC, Dual-Path topology*

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1. INTRODUCTION

With the fast development of modern electronic and communication systems, such as 5G/6G networks, high-speed SerDes interfaces, and digital signal processors (DSPs), there is a growing demand for designs with higher data rates and signal-to-noise ratio (SNR). At the same time, modern integrated circuits (ICs) must meet these strict performance targets with limited power and chip area. In these complex systems, the frequency synthesizer serves as the "heart", which provides the essential periodic clock signals required by different building blocks. For example, it defines the precise sampling time for data converters (ADCs and DACs), synchronizes data flow in digital circuits, and acts as the local oscillator (LO) to perform frequency translation (up and down conversions) in wireless transceivers.

The jitter performance of these synthesized clock signals is extremely important. For instance, the variations of the zero-crossing points directly determines the bit error rate (BER) of communication systems and affects the performance of ADCs. Furthermore, to achieve a large data bandwidth, most modern systems operate in the multi-gigahertz range. The electronics industry also pushes the need for multi-standard transceivers. As a result, the frequency synthesizer must have a wide tuning range to cover different frequency bands and compensate for process, voltage, and temperature (PVT) variations. In addition, the narrow channel spacing in modern communication standards also requires the frequency synthesizer to have a fine frequency resolution.

Over the years, various architectures have been developed to build frequency synthesizers. The main types include direct analog synthesis (DAS), direct digital synthesis (DDS), and indirect synthesis based on the Phase-Locked Loop (PLL) [1, 2]. Although DAS and DDS have their specific uses, PLL-based frequency synthesizers have become the dominant choice in modern IC design. Compared to other methods, PLLs provide a much better trade-off by achieving excellent noise performance with lower power consumption and smaller silicon area. Therefore, designing a high-performance PLL that simultaneously achieves low jitter, low power, and a wide tuning range has became an essential and highly challenging task in today's chip design.

1.1. Traditional Charge-Pump PLL

Over the past few decades, the traditional Charge-Pump PLL (CPPLL) has been the most widely adopted architecture due to its ease of integration and zero steady-state phase error. A standard CPPLL consists of a Phase Frequency Detector (PFD), a Charge Pump (CP), a Low-Pass Filter (LPF), a VCO, and a feedback Divider. However, with the ever-increasing demand for ultra-low jitter, the fundamental architectural flaws of the traditional CPPLL have been increasingly exposed.

To lock the high-frequency VCO signal to a low-frequency reference clock, a frequency divider with a divide ratio of N must be inserted into the feedback loop. In a classical PLL, the main in-band loop noise sources are usually the PD/CP and the divider. Due to the existence of the divide-by-N in the feedback path, the PD/CP and divider noise (in power) is multiplied by N^2 when transferred to the PLL output [3]. As output frequencies push into higher frequencies in modern applications (for example multi-GHz), this problem stated becomes more severe. Consider a output frequency of 2GHz with a reference frequency of 2MHz. The division ratio is set to be 1000. With the division ratio of 1,000, we add 60 dB to the noise from the reference source, the PFD/CP, and the divider when transferred to output, which substantially degrades the in-band phase noise performance. Furthermore, traditional architectures suffer from an inherent trade-off among settling time, spurs, and jitter performance: designers are often forced to sacrifice bandwidth to suppress in-band noise, which in turn slows down the setting time and weakens the loop's ability to suppress the out-of-band noise generated by the VCO, and vice versa. It meets intuition that the PLL achieves optimum jitter performance when its bandwidth is selected to be somewhere near the frequency that the phase noise of free-running VCO is equal to the overall in-band phase noise.

1.2. Sub-Sampling PLL

To break the fundamental bottleneck of the amplification of N^2 noise in traditional CPPLLs, the SSPLL was introduced. The core innovation of the SSPLL is the complete elimination of the frequency divider in the primary phase-locked loop.

Operationally, an SSPLL utilizes a Sub-Sampling Phase Detector (SSPD) to directly sample the high-frequency VCO output voltage waveform via the clean, low-frequency reference clock. Consequently, a high frequency isolation buffer is needed in SSPLL to reduce the kickback noise/charge sharing from SSPD, or it will significantly harm the PLL's spur performance. When the system is in lock, the edges of the reference clock consistently sample near the zero-crossing points of the VCO waveform. Because the high-frequency VCO signal exhibits an exceptionally high voltage slew rate at the zero-crossing points, even a minuscule phase error is converted into a substantial sampled voltage error. This mechanism endows the SSPD with a phenomenally high equivalent phase detection gain.

Due to the absence of a frequency divider and the extremely high phase detection gain, the noise contributions from the CP, when referred to the output, are drastically compressed. Even though the noise from the CP is highly suppressed, the intrinsic noise of the reference clock is still multiplied by a factor of N^2, which now dominates the in-band phase noise. A detailed analysis of the SSPLL noise is demonstrated in the following sections. Additionally, eliminating the divider reduces the overall power consumption of the system, making the SSPLL an ideal candidate for low-power, ultra-low phase noise clock generation.

1.3. Ring VCO Noise Suppression Techniques

Regarding VCO topology selection, the primary candidates are LC Voltage-Controlled Oscillators (LC VCOs) and Ring Voltage-Controlled Oscillators (Ring VCOs). Although LC VCOs utilize passive inductor-capacitor resonant tanks to achieve excellent phase noise, they face severe integration challenges as CMOS technology scales into deep sub-micron nodes (e.g., 28nm and beyond). The silicon area occupied by passive inductors cannot scale proportionally with transistors. Furthermore, LC VCOs inherently suffer from a narrow frequency tuning range, limiting their applicability in wide-band systems.

Compared to LC oscillators, ring oscillators have advantages like more compact chip area, wider frequency tuning range and intrinsic multiphase output signals. However, the inferior jitter/phase noise performance of the ring oscillator is always the bottleneck of the overall PLL jitter/phase noise performance [4].

In order to reduce ring oscillator's phase noise contribution to the overall PLL, several

techniques, such as injection-locked clock multiplier (ILCM) [5], phase noise filter (PNF) [6], feedforward phase noise suppression (FFPNS) [7], and feedback phase noise suppression (FBPNS) [8], are widely researched recently. Although these existing methods can suppress VCO noise, they usually rely on additional circuitry. This extra hardware not only increases the overall design complexity but also occupies a larger silicon area and consumes more power. Therefore, finding a simple and low-power way to suppress VCO noise is highly desired.

Let's consider a simple case where the reference frequency is 20 MHz and the output frequency is 2 GHz (meaning the divide ratio N=100). Typically, the phase noise of a clean reference clock is about -150 dBc/Hz from a few hundred kHz up to over 10 MHz. Due to the N^2 amplification, its noise contribution is raised by 40 dB, resulting in -110 dBc/Hz at the PLL output. In contrast, the phase noise of a low power 2GHz ring VCO is much worse, usually around -90 dBc/Hz at a 1-MHz offset and -115 dBc/Hz at a 10-MHz offset. In order to achieve the optimum phase noise performance, the BW should be selected to be around 5 MHz, if only considering reference clock and VCO. However, the BW of a Type-II PLL is limited to approximately Fref /10 for stability concerns (which is the Gardner's limit) and is often kept smaller than Fref /20 to minimize the REF spurs due to charge pump non-idealities [9]. According to Gardener's theory, it demonstrates that the ratio between the type-II PLL open-loop bandwidth and the reference frequency is theoretically limited by the phase margin. In other words, small ratio between the reference frequency and the open-loop bandwidth will harm the phase margin. Thus, a large enough phase margin should be ensured when the bandwidth is increased [4]. This thesis adopts a high-pass filter in one of the SSCPs' input nodes to widen the bandwidth and at the same time, maintain the phase margin. Meanwhile, a traditional SSCP is connected in parallel with the high pass one to provide normal integration and proportion functions for the loop.

2. PLL MODELING AND NOISE ANALYSIS

2.1. Charge-Pump PLL Basics

While there are many architectures for PLL-based frequency synthesizers, the most widely used one is the charge pump PLL (CPPLL). Therefore, it is essential to introduce the basic structures and have a fundamental understanding of the PLL's operating principles.

As shown in the Fig. **??** below, the loop consists of a VCO of gain K_{vco}[Hz/V], a programmable divider with divider ratio N, a phase/frequency detector (PFD) and a single ended CP with a combined gain of K_{pd} and a low pass filter (LPF) with a trans-impedance $Z_{lf}(s)$.

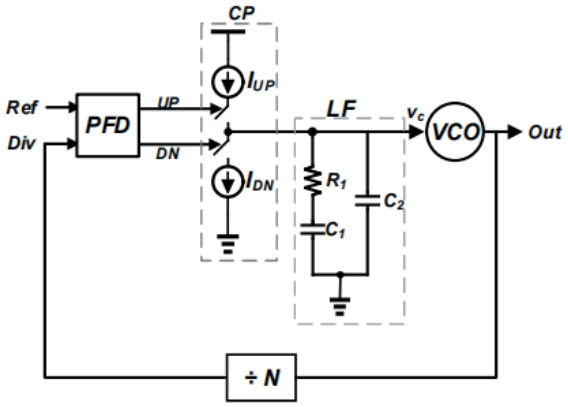

Figure 2.1: loop diagram of a CPPLL

2.1.1. PFD/CP

The PFD/CP often used in PLL design is shown in Fig. 2.2. The reference clock and the divided VCO output signal act as clock signals for two D-flipflops. The PFD generates two pulses, namely UP and DN, to represent the phase difference between the two signals. When UP and DN are both "1", the AND gate generates a "1" and resets both DFF outputs to zero, and that is where the pulses come from.

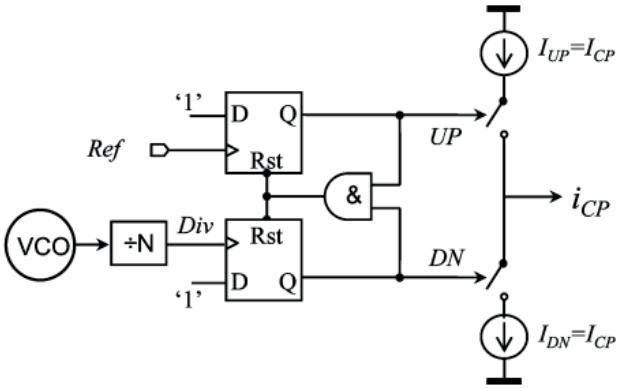

Figure 2.2: Commonly used tri-state PFD/CP (from [3])

Consider a simple case, if the rising edge of the reference signal comes a bit earlier than the feedback signal, the UP signal has a wider pulse. For the same amount of UP and DN current, more current is then injected into the loop filter, resulting in a rise of voltage on the control line. An increased control voltage forces the VCO to operate at a higher frequency. The resulting frequency increase leads to faster phase accumulation, allowing the phase to catch up over time, and eventually eliminate the phase error between reference and feedback signals. In the ideal locked state, the pulse widths for UP and DN signals should be the same, which is approximately equal to the delay of the AND gate. Also, if the delay is too small, then the UP and DN pulse widths will be pretty narrow as well, which does not quite meet the requirement to fully conduct the switches in the following Charge Pump, causing nonlinearity. Meanwhile, the delay for the AND signal of UP and DN should not be too long at the same time. Because longer delay means wider time window for the charge pump to inject noise to the loop, meanwhile degrades the linear detection range when operating at high reference frequencies. At the same time, longer delay means more inverters after the AND gate, consuming more power. A timing diagram of the PFD is shown in Fig. 2.3.

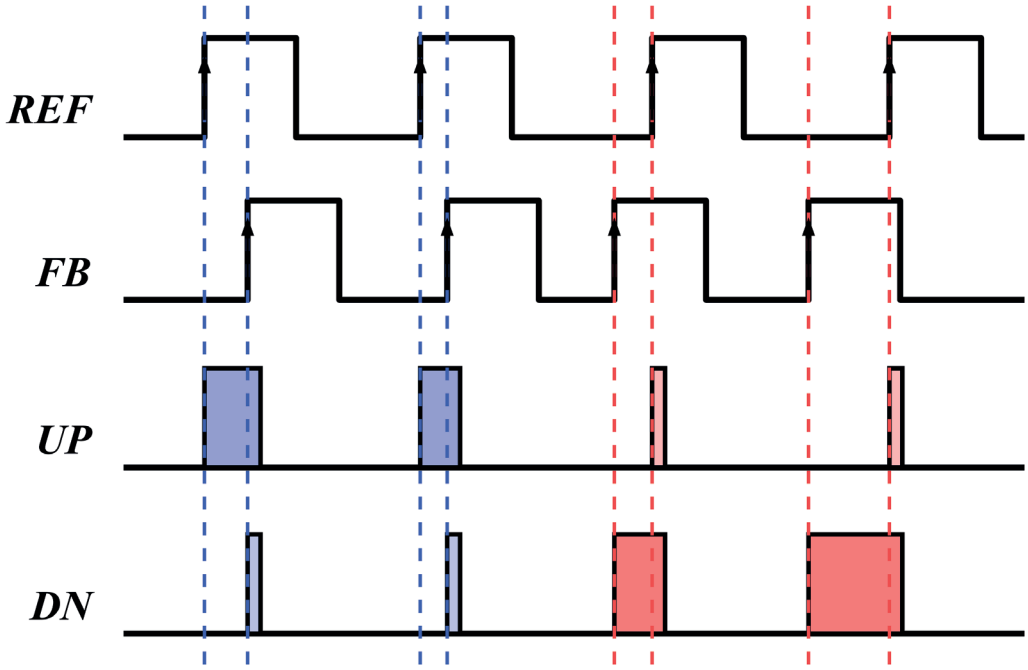

Figure 2.3: timing diagram of a tri-state PFD

The output of the charge pump is proportional to the phase difference between the reference and the feedback signal from the divider. The transfer function of the charge pump is as illustrated below:

$$K_d = \frac{\Delta i_{CP}}{\Delta \phi} = \frac{I_{CP}}{2\pi} \tag{1}$$

As shown in Fig. 2.4, ideally, the charge pump outputs zero static current in locked state, and any phase error at the input is converted into an output current. For example, when the reference signal leads, the phase difference is positive, resulting in a positive output current that drives the VCO to adjust its frequency and phase accordingly.

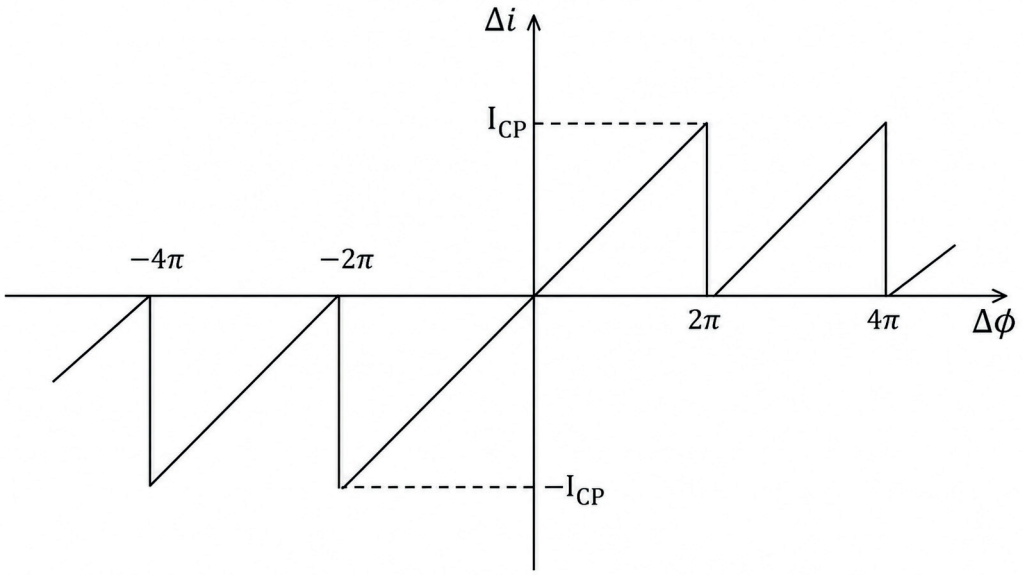

Figure 2.4: PFD/CP characteristics

Here we introduce an analysis to show why CP noise is amplified by a factor of N^2 in CPPLL.

To calculate the CP noise in a PLL system, we usually define a "CP feedback gain." This gain represents the relationship from the PLL output to the CP output current. The concept of CP feedback gain is adopted from [3] and can later show the greatly reduced CP noise in subsampling PLLs in the following sections. The phase domain model is shown below in Fig. 2.5.

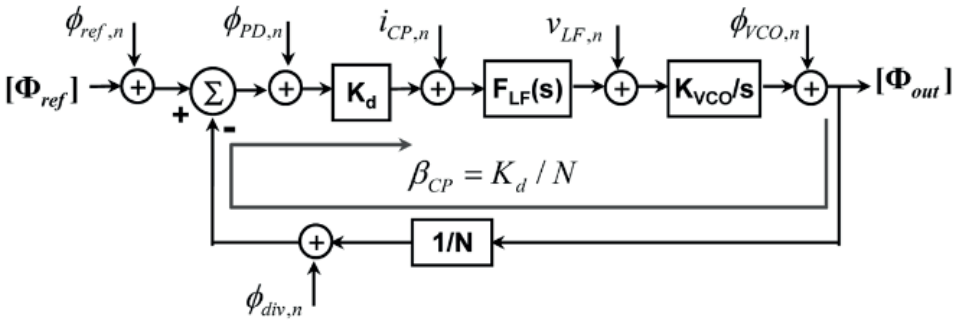

Figure 2.5: Phase domain model for CP feedback gain calculation (from [3])

The transfer function is calculated as follows:

$$H_{CP}(s) = \frac{\phi_{out}}{i_{cp,n}} = \frac{F_{LF}(s) * K_{vco}/s}{1 + K_d * F_{LF}(s) * K_{vco}/s * \frac{1}{N}} \tag{2}$$

$$= \frac{1}{\beta_{cp}} * \frac{H_{openloop}(s)}{1 + H_{openloop}(s)} \tag{3}$$

Since our main concern now is the in-band noise, we have $H_{openloop}(s) \gg 1$, therefore, the noise contributed by CP can be calculated as:

$$\mathcal{L}_{\text{in-band ,CP}} \approx \frac{1}{2} * S_{i\text{CP},n} * |H_{\text{CP}}(s)|^2 \approx \frac{S_{i\text{CP},n}}{2\beta_{\text{CP}}^2} \tag{4}$$

where $S_{i\text{CP},n}$ is the power spectral density of the CP current noise. It is clear that the in-band CP noise is attenuated by a factor of CP feedback gain squared. Therefore, a larger β_{cp} is preferred, as it provides more suppression for CP noise.

Now consider the CP noise in a traditional CPPLL. The CP feedback gain is calculated as follows:

$$\beta_{cp,PFD} = K_d * \frac{1}{N} = \frac{I_{CP}}{2\pi * N} \tag{5}$$

The CP feedback gain is degenerate by the division ratio N, and the current noise is multiplied by a factor of N^2.

2.1.2. LPF

The CP output is fed into the loop filter. In a typical Type-II PLL, the loop filter can be decomposed into two paths, namely the integral path and the proportional-gain path, as shown in Fig. 2.6. The integral path stores the DC component in the LPF. Therefore, in a type I PLL, the only way to provide the DC offset voltage at the input of the VCO is to induce a static phase offset. However, since the VCO itself also acts as an integrator that converts frequency to phase, the overall loop naturally has two integrators. These two integrators will cause a 180-degree phase shift, which makes the feedback loop unstable.

This is exactly why the proportional path is necessary. The proportional path reacts to the immediate phase error and provides a direct, instant voltage adjustment to the VCO. Let's say Δi is generated at the output of the charge pump due to a phase shift of $\Delta\phi$. The voltage deviation on the control line is about $\Delta i * R$, which directly steers the VCO output frequency in the direction that reduces the phase error, improving the transient response of the loop. In the frequency domain, this proportional gain introduces a zero into the open-loop transfer function. This zero provides an essential phase lead to increase phase margin and stabilize the system, preventing the loop from oscillating.

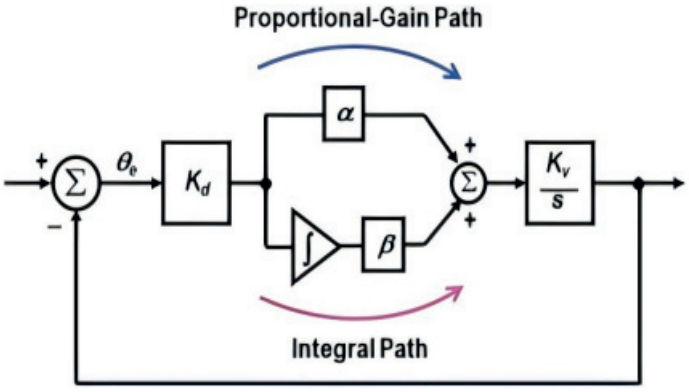

Figure 2.6: Two paths for LPF [10]

We can say that the proportional-gain path is analogous to a small-signal path to set the

gain of an amplifier, while the integral path being analogous to a large-signal path to set the DC operating point of the amplifier [10].

However, for practical usage in a PLL, a simple first order LPF that consists of a capacitor in series with a resistor is not a good solution for a modern PLL, even though first order LPF provides both proportional and integral functions. Simply because, for every comparison cycle of PFD, there is a current pulse coming from the Charge Pump, no matter the CP is charging or discharging the LPF, meaning that there is a periodical voltage ripple caused by the resistor, which is directly connected to the voltage control line. To filter out the ripples, it is important to add another small capacitor connected in parallel with the first order LPF to make it a second order LPF, or the ripples will cause spurs at the PLL output.

Nevertheless, an extra small capacitor connected between voltage control line and ground means an extra weak integrator, which will provide another high frequency pole for the system, and it is needed to be carefully designed to make the high frequency pole slightly larger than the PLL bandwidth to ensure enough phase margin for the loop. Normally, it is practical to set the ratio C1/C2 = 20 or more. The LPF we use in this circuit is shown in Fig. 2.7.

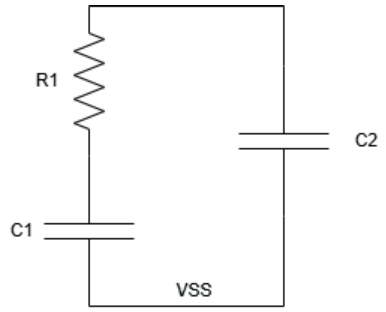

Figure 2.7: typical passive 2nd LPF

2.1.3. VCO

In modern PLL design, the LC VCO is widely used because its passive inductor-capacitor (LC) resonant tank can provide excellent phase noise performance. However, the passive inductor consumes a large chip area, which is difficult to scale down in advanced CMOS

processes. Moreover, LC VCOs usually has a narrow frequency tuning range.

To overcome these physical limitations, the Ring VCO serves as a great alternative. Because it is built entirely using active devices, such as simple inverters or differential delay cells, the Ring VCO requires a significantly smaller area. This makes it extremely easy to integrate into modern dense digital System-on-Chips (SoCs). In addition, the Ring VCO inherently offers a wide frequency tuning range, making it suitable for modern multi-band applications.

A VCO converts an input control voltage into an output frequency. Since phase is the integral of frequency over time, the VCO naturally acts as an ideal integrator in the phase domain. The transfer function of the VCO is calculated as follows:

$$H_{VCO}(s) = \frac{\Phi_{out}(s)}{V_{ctrl}(s)} = \frac{K_{VCO}}{s} \tag{6}$$

where K_{VCO} represents the voltage-to-frequency gain of the VCO, and the $1/s$ term indicates the integration operation. This mathematical model is illustrated by the diagram as shown in Figure. 2.8.

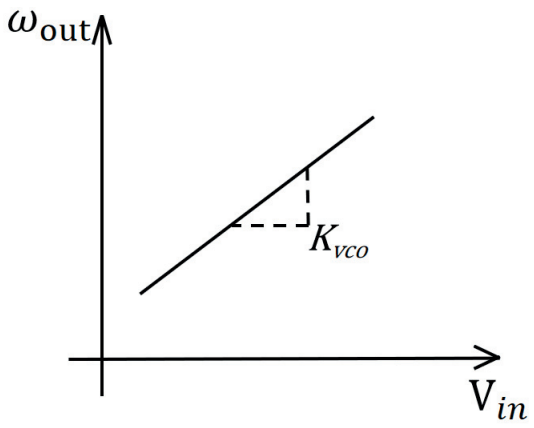

Figure 2.8: VCO transfer function

In this thesis we adopt a current starved Ring VCO. A detailed analysis will be presented

in the following chapters.

2.1.4. Dividers

The output of the VCO is fed to the divider. The divider then divides the high-frequency VCO output signal by a factor of N and generates a lower-frequency feedback clock that can be compared with the reference clock at the PFD. The divider is considered to be in the feedback path in most cases.

With increasing demand of high-speed designs, frequency dividers are required to operate at multi-gigahertz frequencies while dividing the signal down to tens of MHz. This requires a pretty high division ratio. However, directly implementing a fully programmable divider at such high frequencies is challenging. It not only requires complex circuit structures but also consumes an unacceptably large amount of power. To solve this problem, the overall frequency divider is usually split into two parts: a high-speed prescaler and a low-speed programmable digital counter. The prescaler is placed at the front and operates at the VCO output frequency, so it must handle the highest speed in the system. It is usually implemented using fast logic styles such as CML or TSPC and provides a fixed (e.g., divide-by-2 or divide-by-4) or dual-modulus division ratio (e.g., divide-by-4/5). This stage scales the high VCO frequency to a lower range. After that, the remaining division is handled by standard CMOS digital counters, which are more power-efficient. This architecture effectively reduces both design complexity and power consumption of the PLL.

2.2. PLL Loop Noise Analysis

In the previous section we introduced the CP feedback gain to show that the CP noise is multiplied by a factor of N^2. In this section a systematic analysis of the PLL noise component will be presented. It is shown that the PLL loop applies completely different noise-shaping effects to different internal blocks, acting as a low-pass filter for some and a high-pass filter for others.

2.2.1. Out-of-Band Noise

The out-of-band noise is mainly composed of the VCO noise. The Leeson–Cutler phase noise model [11] presents a "basic" model and predicts the phase noise behavior of the free running oscillator; the single sideband to carrier ratio is

$$\mathcal{L}_{VCO}(\Delta f) = 10\log\left\{\frac{2FkT}{P_{sig}}\left[\left(1+\left(\frac{1}{2Q}\frac{f_o}{\Delta f}\right)^2\right)\left(1+\frac{\Delta f_{1/f^3}}{\Delta f}\right)\right]\right\}[dBc/Hz] \qquad (7)$$

where F is an empirical fitting noise factor, k is the Boltzmann constant, T is the absolute temperature, P_{sig} is the power of the oscillator signal, f_0 is the oscillation frequency, Q is the loaded quality factor of the tank, Δf is the offset frequency, and $\Delta f_{1/f^3}$ is the corner frequency between the -30 dB/decade and -20 dB/decade regions in Fig. 2.9.

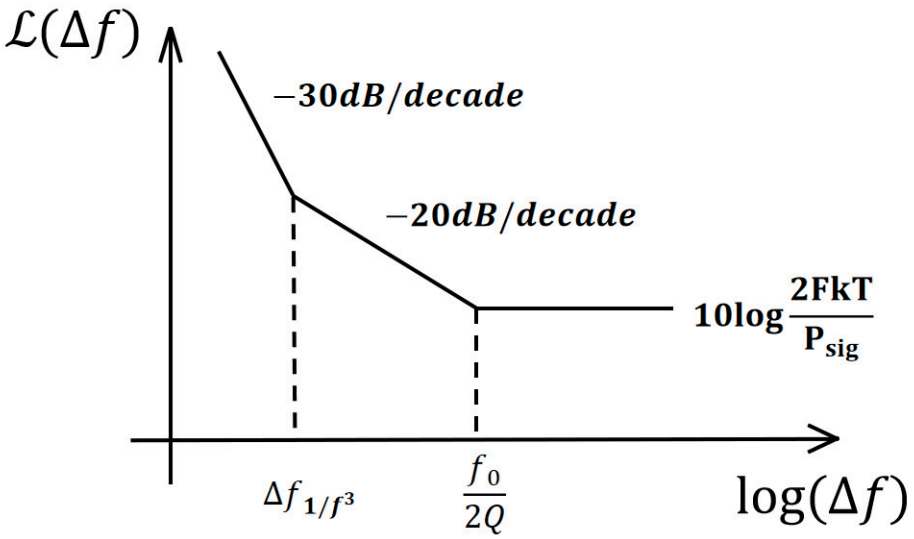

Figure 2.9: Typical phase noise plot of a free running oscillator (Leeson–Cutler model)

It can be deduced from (7) that in order to decrease the phase noise power at a given oscillation frequency f_0 and offset frequency Δf, the signal power and the quality factor Q must be maximized while minimizing the noise factor F.

The transfer function for VCO noise when referred to PLL's output is as follows:

$$H(s)_{VCO} = \frac{1}{1 + K_d * F_{LF}(s) * K_{vco}/s * \frac{1}{N}} \tag{8}$$

The transfer function $H(s)$ behaves like a high-pass filter, and its corner frequency -3 dB f_c determines the noise suppression effect of the PLL on the noise from VCO.

The transfer function of the noise contributed by the loop filter when referring to the output of the PLL is as follows:

$$H(s)_{LF} = \frac{K_{vco}/s}{1 + K_d * F_{LF}(s) * K_{vco}/s * \frac{1}{N}} \tag{9}$$

The noise transfer function from the loop filter when referring to the output of the PLL

behaves like a band-pass filter.

The high-passed noise is as follows:

$$S_{out}(\Delta f) = |H(s)_{VCO}|^2 * S_{vco}(\Delta f) + |H(s)_{LF}|^2 * S_{LF}(\Delta f) \tag{10}$$

The out-of-band noise performance is mainly dominated by the VCO noise, since LPF noise can be made very small.

2.2.2. In-Band Noise

The inband noise is composed of the PFD/CP noise, the reference noise, and the divider noise. In traditional CPPLLs, the PFD/CP noise usually dominates inband noise. As we have discussed in the previous section, the CP noise is multiplied by a factor of N^2. In fact, the noise contributions from the reference clock, the frequency divider, the PD, and the CP can all be referred to the input node of the PD. The CP noise differs from the others only by a scaling factor, i.e., the PD gain, which does not affect the overall noise response of the PLL loop to the noise sources. The CP noise comes from the thermal noise from the current sources. Assume identical I_{UP} and I_{DN}, the charge pump noise is calculated as:

$$S_{CP}(\Delta f) = S_{n,i} = 2 * 4kT\gamma \cdot g_{m,CP} \tag{11}$$

$$= 8kT\gamma \cdot \left(\frac{\alpha I_{cp}}{V_{eff,CP}}\right) \left[A^2/Hz\right] \tag{12}$$

where I_{cp} is the CP current, α is a transistor model parameter, $V_{eff,CP}$ is the effective gate voltage of the transistors in the current source, $g_{m,CP} = \alpha I_{cp}/V_{eff,CP}$ is the equivalent transconductance of the CP current sources, and γ is the noise factor.

In the locked state of the PLL, the CP is only activated for a very short duration T_{PFD} to avoid the dead zone. This is achieved by adding a delay to the PFD reset path, which forces the UP and DN pulses to last for a certain amount of time, which ensures that, ideally, even the smallest amount of phase error is detected. As for noise measurements, this is equivalent to time-domain weighting of the continuous thermal noise. Therefore, the effective noise

power spectral density (PSD) injected into the loop filter should be scaled by the duty cycle, i.e., $T_{\mathrm{PFD}}/T_{\mathrm{ref}}$.

$$S_{out,CP}(\Delta f) = \frac{T_{PFD}}{T_{ref}} * S_{n,i} \tag{13}$$

The transfer function for the CP noise is as follows:

$$H_{CP}(s) = \frac{F_{LF}(s) * K_{vco}/s}{1 + K_d * F_{LF}(s) * K_{vco}/s * \frac{1}{N}} \tag{14}$$

The circuits of the reference path, divider and PFD are digital in nature and operate at the reference frequency f_{ref}. The switching action of these circuits leads to sampling of the phase of the output signal at a rate of f_{ref}. Due to this sampling process, the noise components at frequencies higher than $f_{ref}/2$ are folded back and thus the phase noise spectrum is defined in the Nyquist band $[0, f_{ref}/2]$. Assuming a white noise spectrum, the single-sided phase noise is related to the rms output jitter σ_t as follows [12, 13]:

$$\mathcal{L} = \frac{S_{\phi,n}}{2} = (2\pi\sigma_t)^2 \cdot f_{ref} \left[\mathrm{rad}^2/\mathrm{Hz}\right] \tag{15}$$

The transfer function for PD, divider and reference noise is as follows:

$$H(s) = \frac{Kd * F_{LF}(s) * K_{vco}/s}{1 + K_d * F_{LF}(s) * K_{vco}/s * \frac{1}{N}} \tag{16}$$

$$= N * \frac{LoopGain}{1 + LoopGain} \tag{17}$$

The output inband noise is as follows:

$$S_{out,inband}(\Delta f) = |H(s)|^2 * S_{PFD,divider,ref} + |H_{CP}(s)|^2 * S_{out,CP} \tag{18}$$

3. PROPOSED ARCHITECTURE AND DESIGN TECHNIQUES

As we have discussed in the previous section, Ring VCOs are widely used in today's PLL designs, and we wish to adopt a Ring VCO into our design. To suppress the in-band noise contributed by the VCO, we need a large loop bandwidth. However, a large bandwidth tends to let in more PFD/CP/DIV noise which often dominates in-band noise and therefore jeopardize loop behavior. Also, operating at a high frequency and having a rather low reference frequency demands a frequency divider with a high division ratio. This, in turn, increases the in-band noise, which is undesirable. To break this fundamental trade-off, the SSPLL is introduced as an effective solution [3]. Unlike a traditional CPPLL, the SSPLL completely removes the frequency divider in its main phase-locking path. Instead, it utilizes a sub-sampling phase detector (SSPD) to directly sample the high-frequency VCO waveform using the clean, low-frequency reference clock. When the loop is locked, the sampling instance occurs near the zero-crossing points of the VCO signal. Because the high-frequency VCO waveform has a high slew rate at these points, a tiny phase error is instantaneously converted into a large sampled voltage. This mechanism provides the SSPD with an extremely high phase detection gain [3]. Furthermore, the elimination of the divider inherently avoids the traditional N^2 noise multiplication effect. Consequently, the in-band noise contributed by the phase detector and the charge pump is heavily suppressed. Thanks to these advantages, the SSPLL architecture allows us to safely widen the loop bandwidth to suppress the Ring VCO noise without suffering from severe in-band noise degradation. In this section, we will discuss the proposed SSPLL, the HPF path in SSPD, and the AFC algorithm.

3.1. SSPLL Techniques

The block diagram is shown in Fig. 3.1. The SSPD is the sampler which acts like the phase detector in traditional PLLs. The output of the SSPD is fed into the SSCP, which has a Gm behavior that converts the voltage difference into current difference. This current difference defines the total current injected into or drawn out of the LPF. In ideal locked state, the output current is zero.

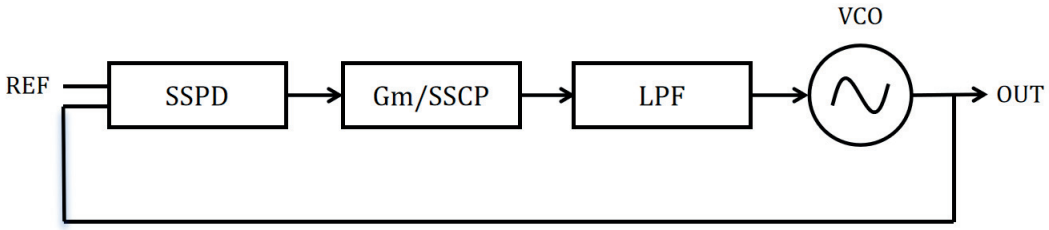

Figure 3.1: SSPLL block diagram

3.1.1. SSPD and SSCP

A Sample-and-Hold (S&H) circuit is cascaded immediately after the sampler, which forms a master-slave S&H structure. It captures the discrete sampled value and maintains it at a constant level throughout the reference period, providing a stable and continuous input for the subsequent transconductor. In [3], a widely used SSPD structure is proposed which is shown below in Fig. 3.2:

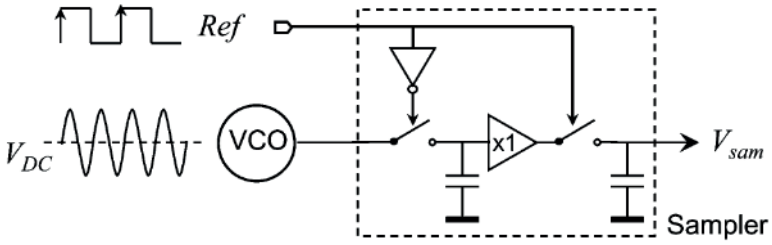

Figure 3.2: Conceptual diagram of sampling based PD [3]

We can see it this way. If we use a single S&H sampler, the output would directly track the high-frequency VCO waveform during the sampling phase. This would cause a large AC ripple to feed into the subsequent transconductor (G_M). The generated current varies drastically, severely modulating the VCO control voltage and creating large spurs. By

adding the slave stage, the output V_{sam} is completely isolated from the VCO's tracking phase. When the master is tracking the VCO, the slave is off, holding the previous voltage. When the master is turned off to hold the new sampled value, the slave turns on to update the output. Consequently, V_{sam} becomes a clean, stable staircase signal that remains constant throughout the entire reference period. Furthermore, the unity-gain buffer inserted between the two stages prevents charge sharing between the two capacitors, ensuring accurate voltage transfer.

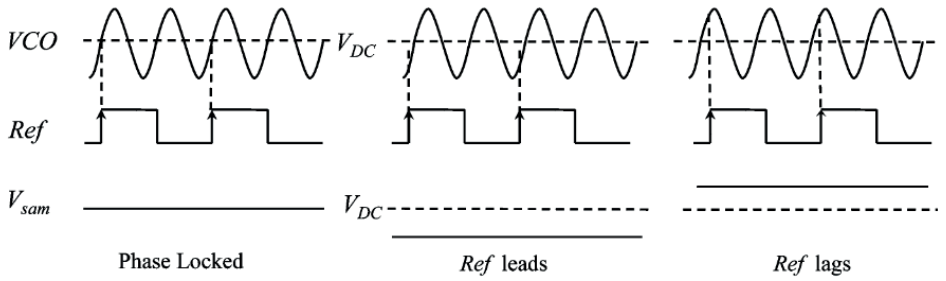

Figure 3.3: Timing diagram of sampling based PD [3]

In Fig. 3.3, the timing diagram of the SSPD is shown to demonstrate 3 cases, namely, phase-locked, ref leads and ref lags. Given that the ratio f_{vco}/f_{ref} is an integer, the sampled voltage V_{sam} is equal to the DC voltage V_{DC} of the VCO signal when the VCO and Ref phases are aligned. If a phase error exists, the difference between V_{sam} and V_{DC} is proportional to the phase error between the VCO and Ref signals. Also, the PD is possible to lock at integer multiples of π, and it cannot differentiate between integer multiples of the reference. Unlike the mixer-based PD, which also exhibits a sinusoidal characteristic, the SSPD is insensitive to the duty cycle or shape of the reference clock, since in each reference period, only a single sample of the VCO phase information is processed [3].

The conceptual diagram of the SSPD/CP is shown below in Fig. 3.4:

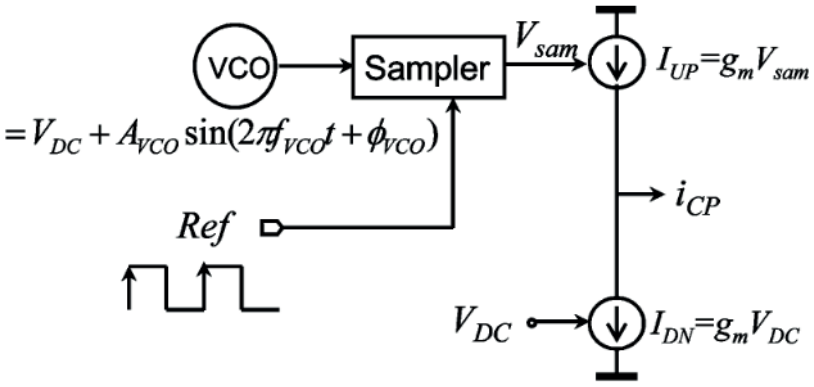

Figure 3.4: Conceptual diagram of SSPD/CP [3]

The DC component of the VCO is fed to the pull-down current source. Vsam is the output of the sampler and is fed to the pull-up current source. The current difference between the two current sources determines the subsequent VCO behavior.

The characteristic of the SSPD/CP is shown below in Fig. 3.5:

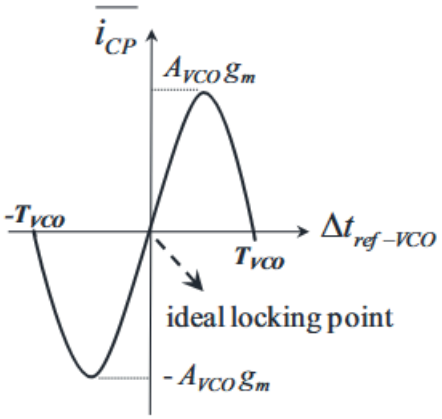

Figure 3.5: Characteristic of SSPD/CP [14]

The ideal locking point is at the zero crossing of the sine wave. However, if there is a

mismatch between the up and down current sources, the loop can lock with a phase error of $\Delta\phi$. Also, note that the characteristic of sampling-based PDs shares the same shape as the VCO waveform. If the VCO waveform is sinusoidal, the PD characteristic is also sinusoidal with a maximum output equal to the VCO peak signal amplitude A_{VCO}. The transfer function of the overall PFD/CP is

$$K_{PD} = \frac{\Delta\overline{i_{CP}}}{\Delta\phi_{VCO}} = \frac{\Delta\overline{i_{CP}}}{\Delta V_{sam}} \cdot \frac{\Delta V_{sam}}{\Delta\phi_{VCO}} = A_{VCO} \cdot g_m \tag{19}$$

If we assume g_m is implemented with a square law MOS transistor in saturation, we can rewrite the equation as:

$$\beta_{CP,SS} = A_{VCO} \cdot g_m = A_{VCO} \cdot \frac{2I_{CP}}{V_{gs,eff}} \tag{20}$$

where $V_{gs,eff}$ is the overdrive voltage of the MOSFET. By comparing the SSPD/CP gain and the PD/CP gain with a tri-state PFD, we can see how the SSPD effectively reduces the CP noise.

$$\frac{\beta_{CP,SS}}{\beta_{CP,PFD}} = N \cdot 4\pi \cdot \frac{A_{VCO}}{V_{gs,eff}}. \tag{21}$$

N is usually a very large number. $4\pi \gg 1$, and in most cases, $A_{VCO} > V_{gs,eff}$. Therefore, the CP gain of the SSPLL is much larger than a traditional CPPLL, thus it has a much higher suppression to the in-band PFD/CP noise.

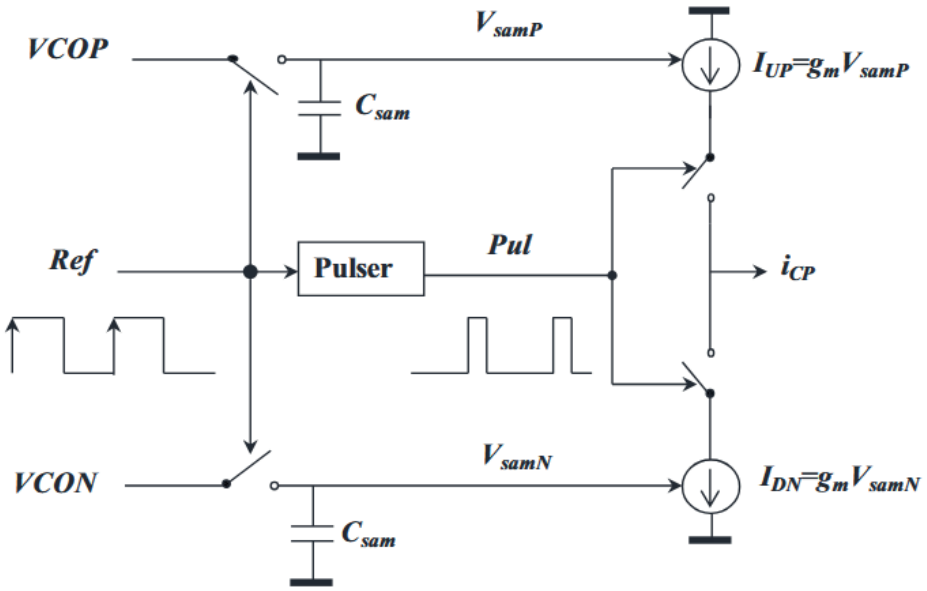

Figure 3.6: SSPD/CP with pulser gain control [14]

3.1.2. SSPD Gain Control

However, this gain is somewhat unnecessarily high. An "unnecessarily high" β_{CP} would not further improve the loop noise but does require a large filter capacitor to stabilize the loop. Fig. 3.6 shows the SSPD/CP with gain control. Differential VCO outputs and differential sampling are used so the differential zero-crossing can naturally be the locking point. Two switches and a block called "Pulser" are added to the CP. The Pulser generates a pulse Pul, non-overlapping with Ref, and switches on/off I_{UP} and I_{DN} simultaneously for a fraction of time τ_{pul} in each T_{ref}. The mean CP output current and thus $\beta_{CP,SS}$ is reduced. Note that switching on the CP only for a fraction of time also reduces CP noise [14]. The overall $\beta_{CP,SS}$ is calculated as:

$$\beta_{CP,SS} = 2A_{VCO} \cdot g_m \cdot \frac{\tau_{pul}}{T_{ref}} \tag{22}$$

The factor of 2 is due to differential sampling. By a careful choice of τ_{pul}/T_{ref}, the

value of $\beta_{CP,SS}$ will not be "unnecessarily high" but just high enough to keep the CP as a negligible contributor to the total loop noise. Note that there are other ways of reducing $\beta_{CP,SS}$, e.g., reducing the sampled voltage slope, reducing g_m by proper sizing/biasing or by adding degeneration [14]. In a conventional sampler, two non-overlapping S&H circuits are required to hold the sampled voltage at a constant DC level, as shown in Fig. 3.2. However, by designing the Pulser to be non-overlapping with the sampling clock Ref, the sampler can be simplified to a single S&H circuit (see Fig. 3.6). In other words, the Pulser fuctions as the slave S&H circuit and the two switches effectively eliminates the need for the second S&H stage. Also, by tuning the pulse width, β_{CP} can be tuned in a wide range without affecting the SSPD/CP operation points [14]. Moreover, employing anti-phase VCO outputs alongside differential sampling effectively mitigates the charge injection and charge sharing problems typically associated with S&H circuits. This fully differential architecture also significantly enhances common-mode supply noise rejection [3].

3.2. SSPLL Noise Analysis

Although sampling based PLLs are discrete time processes in nature, if the sampling period is constant and the open loop bandwidth is constrained to a tenth or less of the sampling rate, the loop behavior can be modeled by using continuous time system approximations [15]. If the system bandwidth constraint is not met, a complete z-domain analysis of the system is required to incorporate the effects of sampling. Due to the sub-sampling operation, the output of the sampler represents an aliased version of the high-frequency VCO signal. The aliased frequency can be expressed as:

$$f_{\text{alias}} = f_{vco} - f_{ref} \cdot \text{round}\left(\frac{f_{vco}}{f_{ref}}\right) = f_{vco} - N \cdot f_{ref} \tag{23}$$

where the round(x) function rounds the value to the nearest integer N. This equation reflects the "virtual multiplication" by N of the reference phase at the phase comparison node. Although this physical frequency multiplication does not exist (since there is no frequency divider in the feedback path), it must be incorporated into the linear phase-domain model to capture its exact effects on the system.

This "virtual multiplication" can be viewed as follows: we are using a low frequency reference to sample a high frequency output, therefore the reference frequency is "virtually multiplied" by N to keep up with the rate of the output frequency. Imagine a phase error $\Delta\phi$ in the reference. The sampling edge is then shifted by

$$\Delta T = \frac{\Delta\phi}{2\pi} \cdot T_{ref} \tag{24}$$

This shift in time domain is certain. However, with a higher frequency, the output signal has a shorter period, which means that this time shift, ΔT, occupies a larger fraction of the total output signal period. The noise referred to the output can be seen as:

$$\Delta\phi_{out} = \Delta T \cdot 2\pi \cdot \frac{1}{T_{out}} \tag{25}$$

$$= N \cdot \Delta\phi \tag{26}$$

Conceptually, the reference phase error is multiplied by N. This reflects the "virtual multiplication" effect.

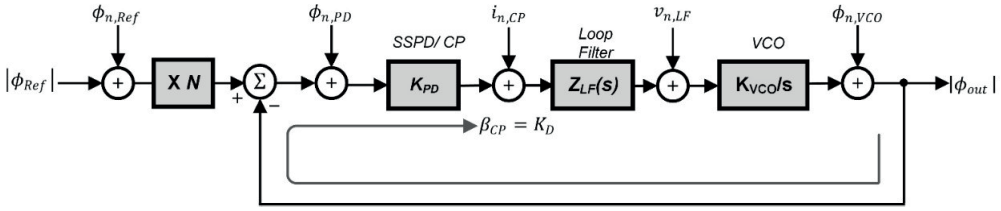

Figure 3.7: Phase domain model of SSPLL with noise sources

Based on the linear model of the SSPLL that is shown in Fig. 3.7, the open-loop transfer function $A_{ss}(s)$ is derived as:

$$A_{ss}(s) = K_{SSPD} \cdot Z_{LF}(s) \cdot \frac{K_{vco}}{s} \tag{27}$$

where K_{SSPD} is the equivalent gain of the sub-sampling phase detector and charge pump, $Z_{LF}(s)$ is the loop filter impedance, and K_{vco} is the VCO tuning gain. Consequently, the closed-loop transfer function $G_{ss}(s)$ from the reference input to the PLL output is given by:

$$G_{ss}(s) = \frac{A_{ss}(s)}{1 + A_{ss}(s)} \tag{28}$$

3.2.1. Out-of-Band Noise

Regarding the noise contributed by the LF and VCO, their physical generation mechanisms in an SSPLL are essentially identical to that in a conventional CPPLL. Because the sub-sampling architecture primarily modifies the phase detection mechanism without altering the forward path of the LF and VCO, their noise models remain unchanged. The transfer function for VCO noise is as follows:

$$H(s)_{VCO,SS} = \frac{1}{1 + K_{SSPD} \cdot Z_{LF}(s) \cdot K_{vco}/s} \tag{29}$$

The transfer function of the loop filter is as follows:

$$H(s)_{LF,SS} = \frac{K_{vco}/s}{1 + K_{SSPD} \cdot Z_{LF}(s) \cdot K_{vco}/s} \tag{30}$$

The high-passed noise is as follows:

$$S_{out}(\Delta f) = |H(s)_{VCO,SS}|^2 * S_{vco}(\Delta f) + |H(s)_{LF,SS}|^2 * S_{LF}(\Delta f) \tag{31}$$

3.2.2. In-Band Noise

The in-band phase noise is mainly composed of the reference noise, the SSPD noise and SSCP noise. Note that the divider noise is eliminated. The fundamental noise limit of the SSPD is bounded by the thermal noise kT/C of the sampling capacitor C_{sam}. In steady-state, the relationship between the total integrated voltage noise variance $\overline{v_{n,SSPD}^2}$ and the corresponding VCO phase error variance is:

$$\overline{v_{n,SSPD}^2} = \frac{kT}{C_{sam}} \approx (A_{VCO} \cdot \Delta\phi_{VCO,SSPD})^2 \tag{32}$$

where A_{VCO} represents the amplitude of the VCO waveform. Due to the aliasing effect of the sampling process, the noise of the SSPD is folded into the Nyquist band $[0, f_{ref}/2]$. Assuming a white noise spectrum, the single-sideband (SSB) in-band phase noise contributed by the SSPD can be integrated over the Nyquist band:

$$(\Delta\phi_{VCO,SSPD})^2 = \int_0^{f_{ref}/2} S_{\phi,SSPD}(f)df = S_{\phi,SSPD}(f) \cdot \frac{f_{ref}}{2} \tag{33}$$

The phase noise PSD of the SSPD is derived as:

$$S_{\phi,SSPD}(f) = \frac{2kT}{C_{sam} \cdot A_{VCO}^2 \cdot f_{ref}} \tag{34}$$

Since $S_{\phi,SSPD}(f)$ is not amplified by N^2 at the PLL output, an excessively large C_{sam} is not required. A moderately sized capacitor is sufficient to keep the SSPD noise contribution negligible, which significantly saves silicon area.

As discussed previously, the SSCP is duty-cycled by the pulser. The current sources are only switched on for a brief fraction of time (τ_{pul}) in each reference cycle (T_{ref}), thereby

minimizing noise injection. The equivalent thermal noise current PSD contributed by the SSCP is formulated as:

$$S_{i,CP} = 2 \cdot 4kT\gamma \cdot g_{m,CP} \cdot \frac{\tau_{pul}}{T_{ref}} \tag{35}$$

where γ is the channel noise factor and $g_{m,CP}$ is the transconductance of the CP transistors. Referring all the noise sources to the input of the SSPD, the equivalent input phase noise PSD can be expressed as:

$$S_{\phi,\text{in}} = N^2 \cdot S_{\phi,Ref} + S_{\phi,SSPD} + \frac{S_{i,CP}}{K_{SSPD}^2} \tag{36}$$

By multiplying this input-referred noise by the closed-loop transfer function $G_{ss}(s)$, the total in-band phase noise PSD at the SSPLL output is:

$$S_{\phi,\text{out}}(\Delta f) = |G_{ss}(j2\pi\Delta f)|^2 \left(N^2 \cdot S_{\phi,Ref} + S_{\phi,SSPD} + \frac{S_{i,CP}}{K_{SSPD}^2} \right) \tag{37}$$

The noise contributions from the SSPD and CP are not multiplied by N^2 when transferred to the output. However, the noise from the reference clock and its buffers still suffers from the N^2 amplification, which now is more likely to dominate in-band noise. Overall, the SSPLL architecture achieves significantly lower in-band noise compared to traditional divider-based PLLs.

Despite its attractive noise benefits, the discrete sampling nature of the SSPD and the low frequency of the reference clock introduce a critical drawback: the SSPLL is prone to false locking onto other integer harmonics. It is not that the SSPLL cannot lock the output frequency f_{out} exactly to $N \cdot f_{ref}$, but rather it cannot distinguish the target frequency $N \cdot f_{ref}$ from adjacent harmonics, such as $(N \pm 1) \cdot f_{ref}$.

Because the SSPD acts solely as a phase detector without any frequency discrimination capability, it will yield a steady zero-error voltage as long as the reference edges align with the zero-crossings of the VCO waveform, regardless of the specific harmonic frequency. The SSPLL suffers from the narrow linear range in the PD characteristic and requires good frequency acquisition with additional circuitry [10], e.g., a frequency-locked loop (FLL). This auxiliary loop is responsible for bringing the initial VCO frequency sufficiently close to the target before engaging the main sub-sampling loop.

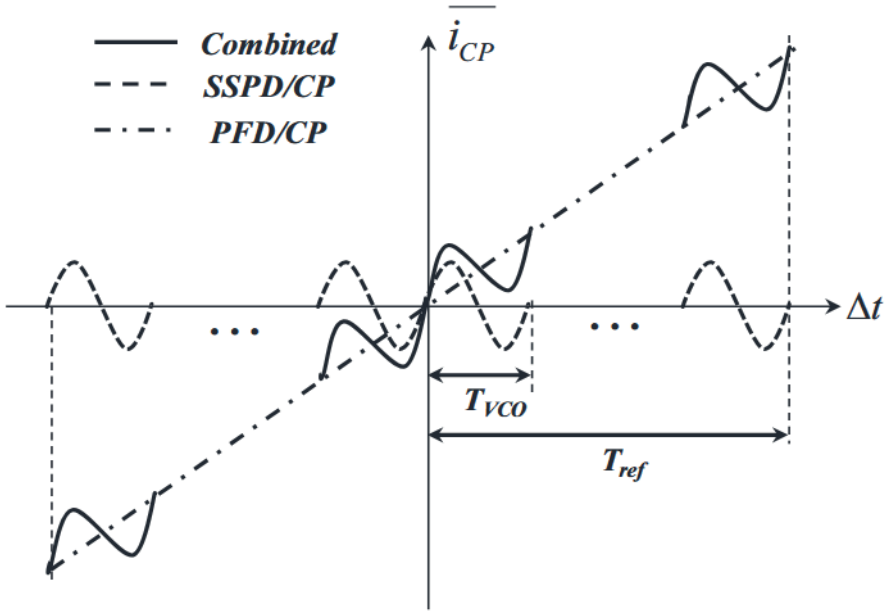

Figure 3.8: Combined SSPD/CP and PFD/CP characteristic [14]

To ensure a smooth transition from frequency acquisition to phase locking, a dead-zone (DZ) is introduced in the auxiliary FLL. When the VCO frequency is far from the target $N \cdot f_{ref}$, the large phase error lies outside the DZ. The FLL is then dominant and pulls the frequency towards the target.

As the frequency error decreases, the phase error enters the DZ, and the FLL CP outputs zero current. The FLL is thus disabled and the sub-sampling loop takes over to finalize phase locking. To avoid false triggering by noise, the DZ is designed to be larger than the maximum steady-state VCO jitter. As a result, the FLL remains inactive in the locked state, ensuring no degradation in jitter performance.

Actually, the work in [16] shows that the loop would also work without a DZ, since around the locking point $\beta_{CP,SS}$ can be much larger than $\beta_{CP,PFD}$ anyway. The overall characteristic of the combined SSPD/CP and PFD/CP is shown in Fig. 3.8

With no DZ, the PFD/CP in the FLL will inject noise even in the locked condition. As discussed previously, the noise contributions from the PFD, CP, and divider in the auxiliary loop are amplified by a factor of N^2 due to the division ratio. However, in the locked state, the SSPLL dominates the loop, and its large phase detector gain effectively suppresses the CP noise of the auxiliary loop, while the other noise sources are negligible. Therefore, even without deadzone, the auxiliary loop noise has negligible impact on the overall in-band phase noise, since it is attenuated by a factor of $(\beta_{CP,SS} + \beta_{CP,PFD})^2$. After locking, the FLL can be disabled to save power, or it can remain active to continuously monitor the phase/frequency error and improve the SSPLL's robustness against disturbances [14, 16]. In this design, we implemented the DZ anyway to save power.

3.4. Dual-path Architecture

The previous descriptions of the SSPLL characteristics, SSPD gain control, noise analysis, and the auxiliary FLL are all based on [3]. This represents the classic SSPLL architecture.

Building on this foundation, this section introduces a dual-path SSCP, which adds a high-pass filter at a specific node to increase the loop bandwidth. The block diagram of the proposed SSPLL is shown in Fig. 3.9.

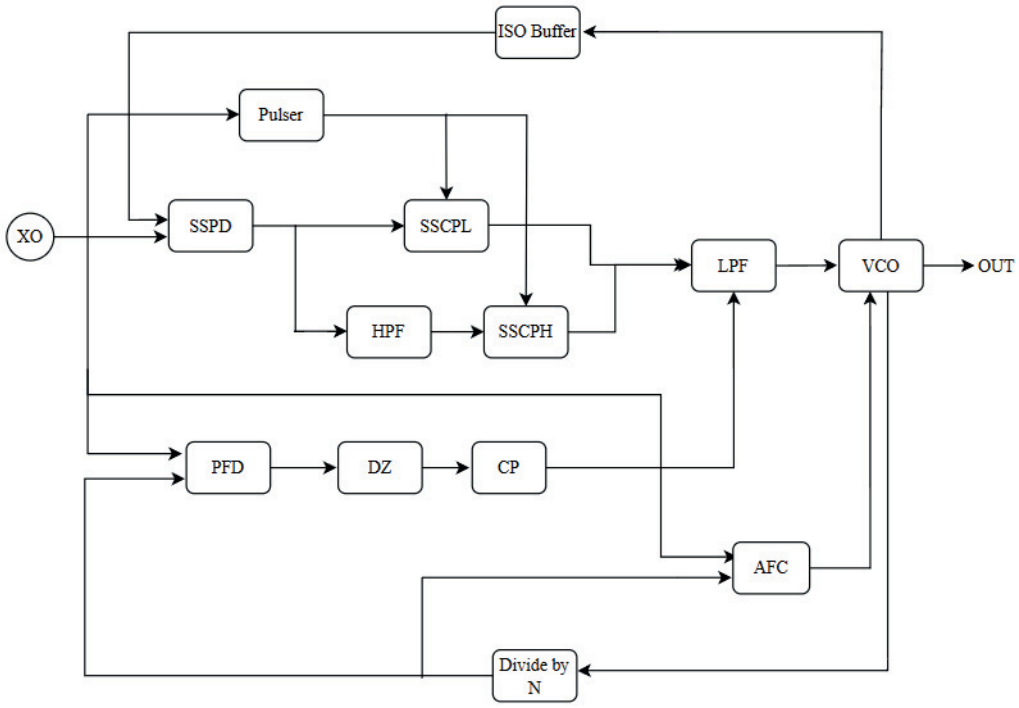

Figure 3.9: Block diagram of the proposed SSPLL

For the proposed dual-path SSPL, one path from the SSPD to the LPF is through SSCPL, and the other path is composed of the HPF and SSCPH. These two paths are operating simultaneously to control the current injected into the LPF. Through properly setting the HPF's high-pass frequency corner and SSCPs' transconductances, a new in-band zero and

pole are generated to enlarge the PLL bandwidth. Moreover, since the frequency of the introduced zero is smaller than the pole, the phase margin of the PLL can be compensated. As a consequence, the phase noise of the ring VCO can be suppressed while the loop stability is still ensured.

The circuit implementation is shown below in Fig. 3.10 to aid further understanding of the impact of the HPF on loop transfer function and bandwidth extension.

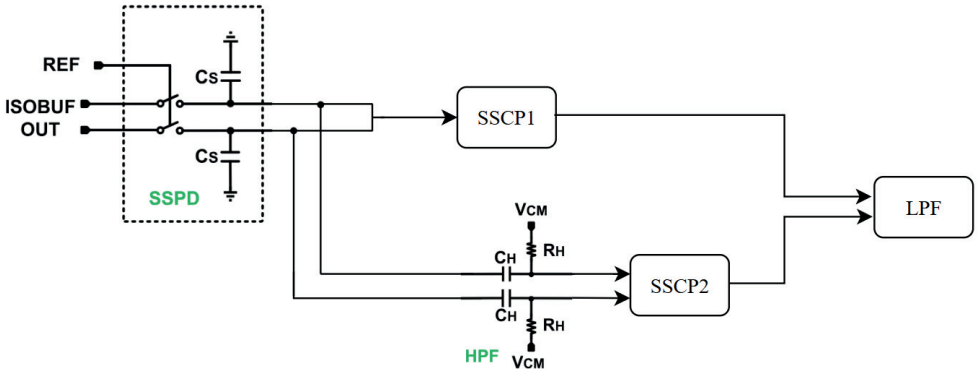

Figure 3.10: Circuit implementation of the HPF

Based on the dual-path topology, the combined phase-domain transfer function of the SSPD and the SSCPs is approximated as follows:

$$H_{\mathrm{PD\&CP}}(s) \cong 2A_{\mathrm{ISOBUF}} \cdot \left(g_{m,\mathrm{SSCP1}} + \frac{R_H C_H s}{1 + R_H C_H s} \cdot g_{m,\mathrm{SSCP2}} \right) \cdot \frac{\tau_{\mathrm{PUL}}}{T_{\mathrm{REF}}} \tag{38}$$

In this expression, A_{ISOBUF} is the signal amplitude at the ISOBUF output. The parameters $g_{m,\mathrm{SSCP1}}$ and $g_{m,\mathrm{SSCP2}}$ are the transconductances of SSCP1 and SSCP2, respectively. τ_{PUL} defines the pulse width of the pulser signal, and T_{REF} (which corresponds to $1/f_{\mathrm{REF}}$) stands for the reference clock period.

Now we have a new zero and a new pole generated respectively at:

$$f_{\mathrm{ZF}} = \frac{g_{m,\mathrm{SSCP1}}}{2\pi(g_{m,\mathrm{SSCP1}} + g_{m,\mathrm{SSCP2}})R_H C_H} \tag{39}$$

$$f_{\mathrm{PF}} = \frac{1}{2\pi R_H C_H} \tag{40}$$

It is clear that the zero frequency is smaller than the pole frequency, and the ratio of them is decided by two SSCPs' transconductances. From a control perspective, this strategically placed lower-frequency zero provides a phase lead to stabilize the wideband loop, while the higher-frequency pole is pushed further away to prevent phase margin degradation. This tunability allows the PLL to achieve bandwidth extension without sacrificing overall loop stability.

The conceptual open-loop gain of the conventional SSPLL and the dual-path SSPLL is shown in Fig. 3.11 and Fig. 3.12

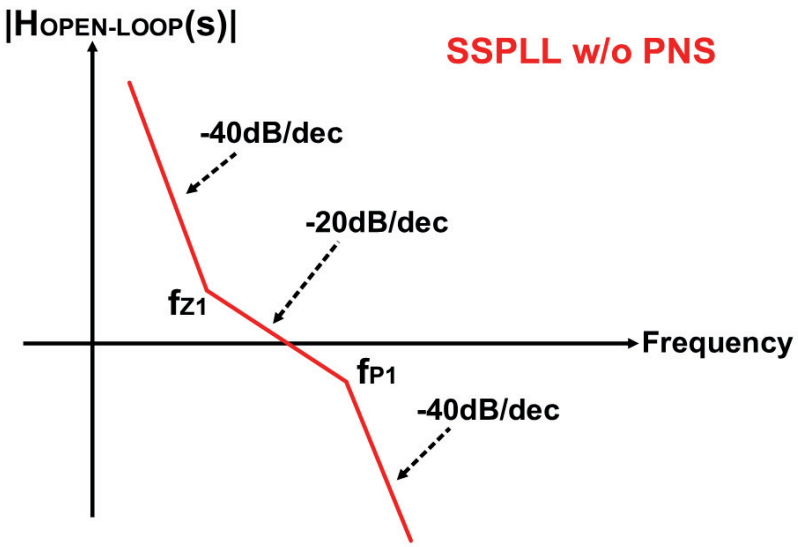

Figure 3.11: Conceptual open-loop gain of Conventional SSPLL [4]

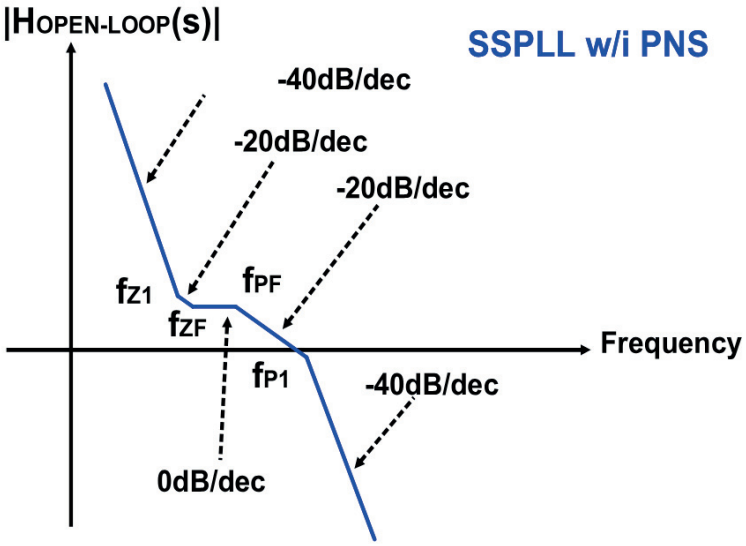

Figure 3.12: Conceptual open-loop gain of Dual-path SSPLL [4]

For the conventional type-II SSPLL, the slope of the open-loop gain is changed from -40 to -20 dB/dec at the first zero f_{Z1}, and then from -20 to -40 dB/dec at f_{P1}. The open-loop gain of the dual-path structure has different characteristics. The slope is first changed from -40 to -20 dB/dec at f_{Z1} and then to 0 dB/dec at the new zero f_{ZF}. After that, the slope begins to reduce to -20 dB/dec when it encounters the newly-implemented pole f_{PF} and finally reduces to -40 dB/dec due to the pole f_{P1}. From the conceptual open-loop gain, it can be seen that the open-loop bandwidth is obviously extended and the expansion effect is decided by f_{ZF} and f_{PF}.

In Matlab modeling, we have the BW and phase margin of the open loop with and without the HPF path to be:

Table I: Open-loop bandwidth and phase-margin comparison with and without the HPF path

Case	**UnityGainBW_MHz**	**PhaseMargin_deg**
With HPF dual path	5.45	67.467
Without HPF path	4.7815	61.852

Since the dual-path architecture is based on the conventional SSPLL architecture, there is not much difference in phase noise performance. The main difference lies within the SSPD&SSCP noise.

The PD noise is varied due to the HPF. To analyze the extra noise generated by the HPF, we perform the following calculations. Fig. 3.13 illustrates the noise equivalent circuits of the SSPD and HPF during the sampling process. The variables V_{N1} and V_{N2} denote the noise voltages at the intermediate sampling node and the HPF output node, respectively. These noise components are then injected into the 2 SSCPs and transferred to the PLL output.

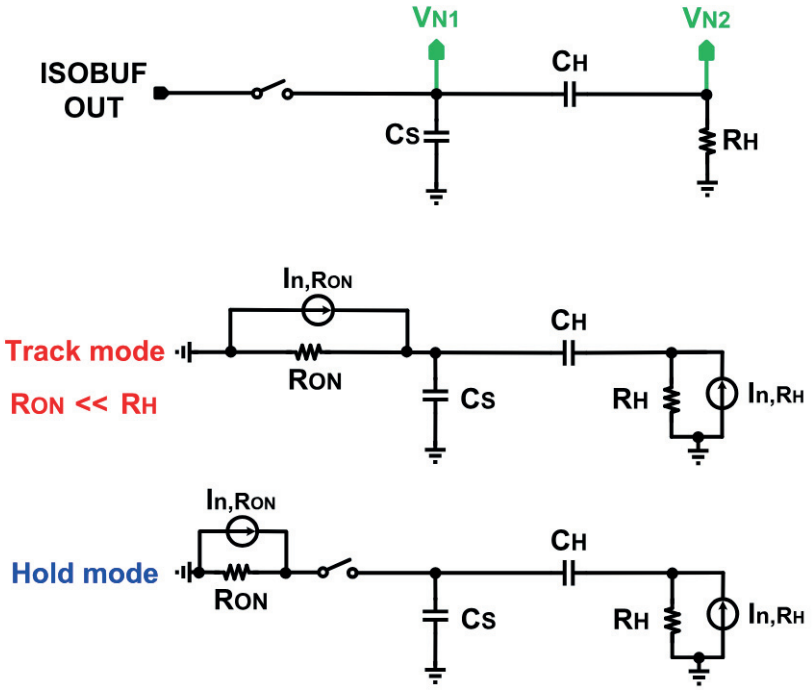

Figure 3.13: Noise analysis of the SSPD and HPF [4]

To accurately calculate the noise spectrum at V_{N1}, we must treat the switched-capacitor network as a linear periodically time-varying (LPTV) system. In such systems, the total baseband noise is the superposition of three parts: track-mode noise, hold-mode noise, and

their cross-correlated noise.

During the track mode (switch turned on, $R_{\mathrm{ON}} \ll R_{\mathrm{H}}$), the broadband thermal noise from R_{H} and R_{ON} is modulated by the sampling clock. Acting as a square-wave mixer, the clock folds the high-frequency noise back into the baseband through its odd harmonics (e.g., fundamental and 3rd harmonic, whereas higher-order harmonics are negligible). To prevent double-counting, the highly correlated low-frequency noise of R_{ON} is deliberately excluded from this specific tracking calculation. The single-sided PSD for the track mode is derived as:

$$S_{VN1\_T} \cong 4 \cdot \left(2kTR_{\mathrm{ON}} + \frac{2kT}{R_{\mathrm{H}}} \cdot R_{\mathrm{ON}}^2 \right) \cdot \left(\frac{1}{\pi^2} + \frac{1}{9\pi^2} \right) \tag{41}$$

During the hold mode (switch turned off), the noise spectrum originates from two mechanisms. The first part is the broadband noise of R_{ON} sampled onto the capacitor, which mathematically equals impulse-sampled noise convolved with a hold-duration square pulse (resulting in a sinc-shaped spectrum). The second part is the continuous thermal noise of R_{H} directly modulated by the reference signal. Thus, the hold-mode PSD is expressed as:

$$S_{VN1\_H} \cong 2kT \cdot \left(\frac{1}{4C_{\mathrm{EQ}} f_{\mathrm{REF}}} - \frac{R_{\mathrm{ON}}}{2} \right) + 8kTR_{\mathrm{H}} \cdot \left(0.25 + \frac{1}{\pi^2} + \frac{1}{9\pi^2} \right) \tag{42}$$

where C_{EQ} represents the equivalent capacitance seen at the node, and its effective value lies between C_{S} and $C_{\mathrm{S}} + C_{\mathrm{H}}$.

The cross-correlated noise between the track and hold modes (mainly derived from the low-frequency continuous noise) is evaluated separately as:

$$S_{VN1\_R} \cong 4kTR_{\mathrm{ON}} \tag{43}$$

Consequently, the total one-sided noise PSD at V_{N1} is simply the linear sum of these three independent calculations:

$$S_{VN1} = S_{VN1\_T} + S_{VN1\_H} + S_{VN1\_R} \tag{44}$$

The noise spectrum at node V_{N2} can be analyzed using the same method. In the track mode, both R_{ON} and R_{H} generate noise. Their low-frequency components are accounted for as

correlated noise, and the higher-order noise from R_{H} is attenuated by the inherent bandwidth limitation. Therefore, the track-mode noise at V_{N2} is dominated by the modulated R_{ON} noise:

$$S_{VN2\_T} \cong 8kTR_{\mathrm{ON}} \cdot \left(\frac{1}{\pi^2} + \frac{1}{9\pi^2}\right) \tag{45}$$

For the hold-mode noise at V_{N2}, the sampled R_{ON} noise behaves identically to that at V_{N1}. The contribution from R_{H} is deduced by convolving its high-order noise with the square-wave reference clock. The total hold-mode PSD at V_{N2} is formulated as:

$$S_{VN2\_H} \cong 2kT \cdot \left(\frac{1}{4C_{\mathrm{EQ}}f_{\mathrm{REF}}} - \frac{R_{\mathrm{ON}}}{2}\right) + 8kTR_{\mathrm{H}} \cdot \left(\frac{1}{\pi^2} + \frac{1}{9\pi^2}\right) \tag{46}$$

Similarly, the related noise component at node V_{N2} originates from the continuous, unmodulated low-frequency thermal noise of both R_{ON} and R_{H}. Its one-sided PSD is evaluated as:

$$S_{VN2\_R} \cong 4kT(R_{\mathrm{ON}} + R_{\mathrm{H}}) \tag{47}$$

The overall one-sided noise PSD at node V_{N2} is derived as:

$$S_{VN2} = S_{VN2\_T} + S_{VN2\_H} + S_{VN2\_R} \tag{48}$$

The transfer function from $VN1$ to output is derived as:

$$H_{VN1}(s) = \frac{g_{m,\mathrm{SSCP1}} \cdot \frac{\tau_{\mathrm{PUL}}}{T_{\mathrm{REF}}} \cdot Z_{LF}(s) \cdot \frac{K_{\mathrm{VCO}}}{s}}{1 + A_{ss}(s)} \tag{49}$$

The transfer function from $VN2$ to output is derived as:

$$H_{VN2}(s) = \frac{\frac{R_{\mathrm{H}}C_{\mathrm{H}}s}{1+R_{\mathrm{H}}C_{\mathrm{H}}s} g_{m,\ \mathrm{SSCP2}} \cdot \frac{\tau_{\mathrm{PUL}}}{T_{\mathrm{REF}}} \cdot Z_{LF}(s) \cdot \frac{K_{\mathrm{VCO}}}{s}}{1 + A_{ss}(s)} \tag{50}$$

The output noise is calculated as:

$$S_{out,SSPD}(\Delta f) = S_{VN1} \cdot |H_{VN1}(s)|^2 + S_{VN2} \cdot |H_{VN2}(s)|^2 \tag{51}$$

The noise contributed by the SSPD and HPF should be around $-130dBc/Hz$.

The charge-pump is viewed as a V-I converter as usual. The generated current noise is determined by their respective transconductances. Consequently, the spectrum of the thermal noise current can be expressed as:

$$S_{\mathrm{SSCP},n} = 4kT\gamma\frac{\tau_{\mathrm{PUL}}}{T_{\mathrm{REF}}}\left(g_{m,\mathrm{SSCP1}} + g_{m,\mathrm{SSCP2}}\right) \tag{52}$$

The transfer function of the SSCP is calculated as follows:

$$H_{SSCP}(s) = \frac{Z_{LF}(s)\cdot\frac{K_{VCO}}{s}}{1 + A_{ss}(s)} \tag{53}$$

The output noise of the SSCP is calculated as follows:

$$S_{out,SSCP}(\Delta f) = S_{SSCP,n}\cdot|H_{SSCP}(s)|^2 \tag{54}$$

With careful control of the pulse width τ_{PUL}, the SSCP noise can be as low as $-135dBc/Hz$.

3.5. AFC Algorithm

To cover a wide frequency range from 2 GHz to 4 GHz, a Ring VCO requires a large tuning capability. If the design relies on a single continuous tuning control line, the VCO gain (K_{VCO}) must be extremely high. A high K_{VCO} makes the oscillator highly sensitive to the ripple on control line, which degrades the phase noise performance. To solve this issue, the total tuning range of the VCO is typically divided into multiple overlapping discrete frequency bands (for instance, by switching capacitor banks or discrete current branches). The implementation is conceptually demonstrated in Fig. 3.14.

This is where the Automatic Frequency Calibration (AFC) algorithm is introduced. The AFC is a digital control block. Its primary function is to compare the VCO frequency with the reference clock and automatically select the most appropriate discrete frequency band for a given target frequency. By implementing this digital coarse tuning, the continuous tuning path only needs to cover a narrow frequency range within the selected band. This allows for a much lower K_{VCO}, which leads to better noise performance.

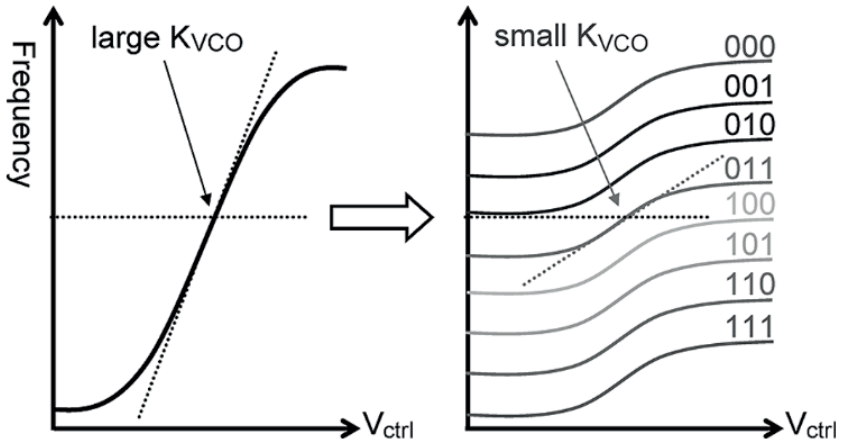

Figure 3.14: Technique for reducing the VCO tuning gain [17]

In the proposed dual-path SSPLL architecture, an auxiliary FLL with a dead zone is already utilized to assist the sub-sampling loop in frequency acquisition. One might ask why an AFC algorithm is still necessary when an FLL is present. The answer lies in the wide operation range and the required locking speed.

The FLL is an analog feedback loop. When the PLL is required to perform a large frequency jump, such as from 2 GHz to 4 GHz, the charge pump in the FLL needs to charge or discharge the large loop filter capacitor across a wide voltage range. This analog integration process takes a long time. Furthermore, the target frequency might physically fall outside the coverage of the currently active discrete band, making it impossible for the analog FLL to lock without a band switch.

By incorporating the AFC algorithm, the locking process is systematically divided into three efficient stages. First, the digital AFC quickly switches the VCO to the correct discrete band. Once the AFC finishes its operation, the frequency error is already minimized to a narrow window. Second, the analog FLL takes over to pull the frequency into the designed dead zone. Because the AFC has already brought the frequency close to the target, the FLL requires less time to charge the loop filter. Finally, the FLL turns off, and the core sub-sampling loop takes over to achieve precise phase locking. In summary, the AFC acts as

a fast digital preliminary step. It cooperates with the analog FLL to guarantee fast locking across the entire frequency range.

3.5.1. Basic Operation

The purpose of performing VCO calibration is to determine an optimum VCO sub-band under which the PLL can acquire locking to a reference signal properly. During calibration, comparisons between the VCO frequency and the reference frequency are performed. The frequency comparisons can be carried out when the PLL loop is either open or closed. Therefore, the VCO calibration techniques can be categorized into two types according to the PLL status during calibration [17].

The block diagrams of the two methods are illustrated in Fig. 3.15 and Fig. 3.16

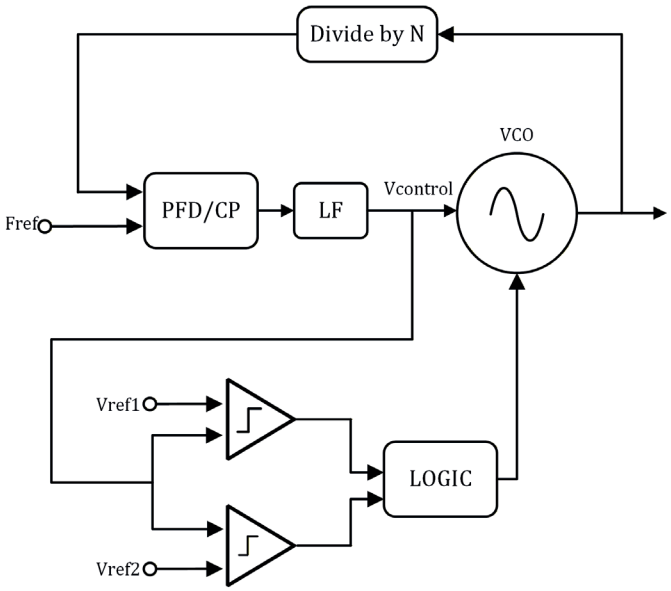

Figure 3.15: Conventional closed-loop VCO calibration technique

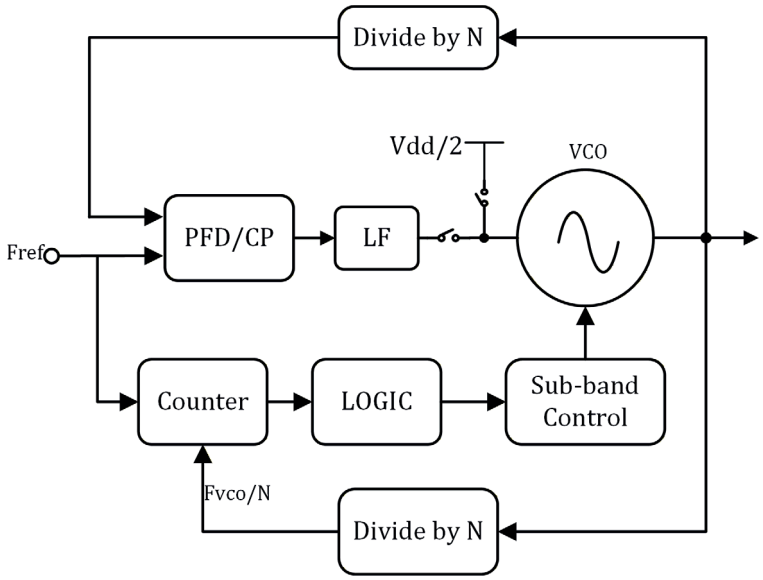

Figure 3.16: Conventional open-loop VCO calibration technique

In the closed-loop VCO calibration approach, the PLL remains fully connected and repeatedly attempts to lock under different VCO sub-band settings. The system determines the correct sub-band by checking whether the settled control voltage (V_{ctrl}) falls within a predefined reference voltage window. However, this method is inherently slow because the entire PLL must be settled before each valid voltage comparison can be executed.

Alternatively, the open-loop calibration method disconnects the loop filter and fixes V_{ctrl} to a constant reference voltage, typically $V_{\text{dd}}/2$. It evaluates the frequency error by utilizing digital counters to simultaneously count the reference clock and the divided VCO signal cycles. Unfortunately, to minimize initial phase uncertainties and guarantee calibration accuracy, the counters must accumulate a massive number of cycles, which makes this process also slow.

The AFC technique adopted in this thesis is based on the Time-to-Voltage Converter (TVC) calibration method proposed in [17]. This approach circumvents the calibration time limitations caused by either PLL settling behavior or long cycle counts. Therefore, it is helpful to first review the basic operation of this TVC-based structure. Following this background,

the next section will detail how our implemented AFC operates.

The block diagram of the TVC-based calibration technique is as shown in Fig. 3.17.

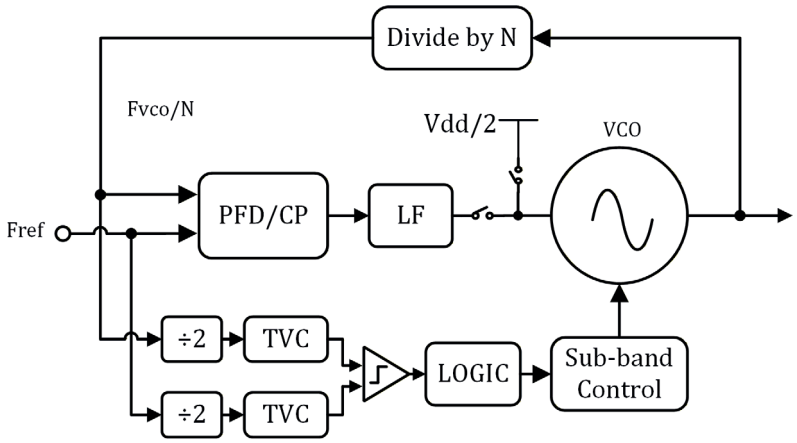

Figure 3.17: TVC-based agile VCO calibration technique

This approach compares two signal frequencies is to directly measure their periods in the time domain using TVCs. In this architecture, divide-by-2 circuits are first utilized to ensure the input signals have a strict 50% duty cycle, allowing the pulse width to represent the full signal period T_{REF}. The TVC then translates this time duration into a voltage quantity. The TVC is shown in Fig. 3.18, which can be implemented using a charge pump and a peak detector. During the positive half-cycle, the capacitor C_1 is linearly charged by a constant current I_1, reaching a peak voltage formulated as:

$$V_{1,\max} = \frac{T_{\mathrm{REF}} \cdot I_1}{C_1} \tag{55}$$

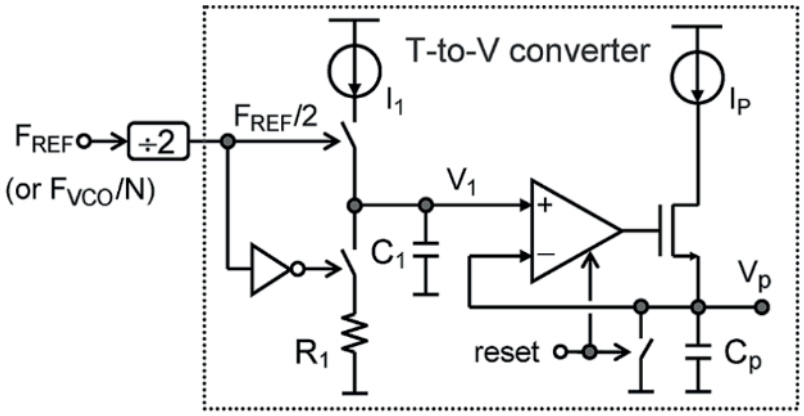

Figure 3.18: TVC circuit [17]

The peak detector stores this maximum voltage ($V_{\mathrm{p}} = V_{1,\max}$) for the voltage comparator. Since this charging process takes only a few reference cycles, the calibration is very fast. It effectively avoids the long PLL settling time and the large cycle counting required by traditional methods. After the state machine uses the comparison result to adjust the VCO sub-band, a reset signal discharges the peak detector to get ready for the next cycle.

Essentially, this technique performs an absolute period measurement followed by a relative voltage comparison. Assuming the TVC is designed to map the nominal period T to a common-mode voltage V_{ref} (i.e., $T \cdot I_1/C_1 \cong V_{\mathrm{ref}}$), the voltage difference at the comparator input for a given period error ΔT is derived as:

$$\Delta V_{\mathrm{comp}} = (T + \Delta T)\frac{I_1}{C_1} - T\frac{I_1}{C_1} = \Delta T\frac{I_1}{C_1} \cong V_{\mathrm{ref}}\left(\frac{\Delta T}{T}\right) \tag{56}$$

While this open-loop time-domain comparison is extremely fast, the equation above exposes its bottleneck: the calibration accuracy is heavily restricted by analog imperfections. For instance, achieving a 1% frequency resolution with a 1.5-V V_{ref} implies that the total circuit error must be kept below 15 mV. Any physical mismatch between the two TVC paths (such as variations in charge pump currents, sampling capacitors, and peak detectors) or the intrinsic offset of the comparator will easily swallow this tiny voltage margin, leading to false

frequency locking.

To alleviate the constraints imposed by mismatch, a relative comparison is introduced to replace absolute measurements. Two TVCs are replaced by a dual-edge phase detector and a charge pump, which generate pulses on both the rising and falling edges. The VCO rising edge is intentionally arranged to occur earlier than the reference edge. By comparing the widths of the UP and DN pulses, it is then possible to determine which signal has the longer period, and therefore the lower frequency. With this approach, the requirements on device matching and comparator offset are relaxed, while the hardware cost is also reduced. As this topic is beyond the main scope of this thesis, it will not be discussed in further detail here. The operation timing diagram of the relative measurement is shown in Fig. 3.19.

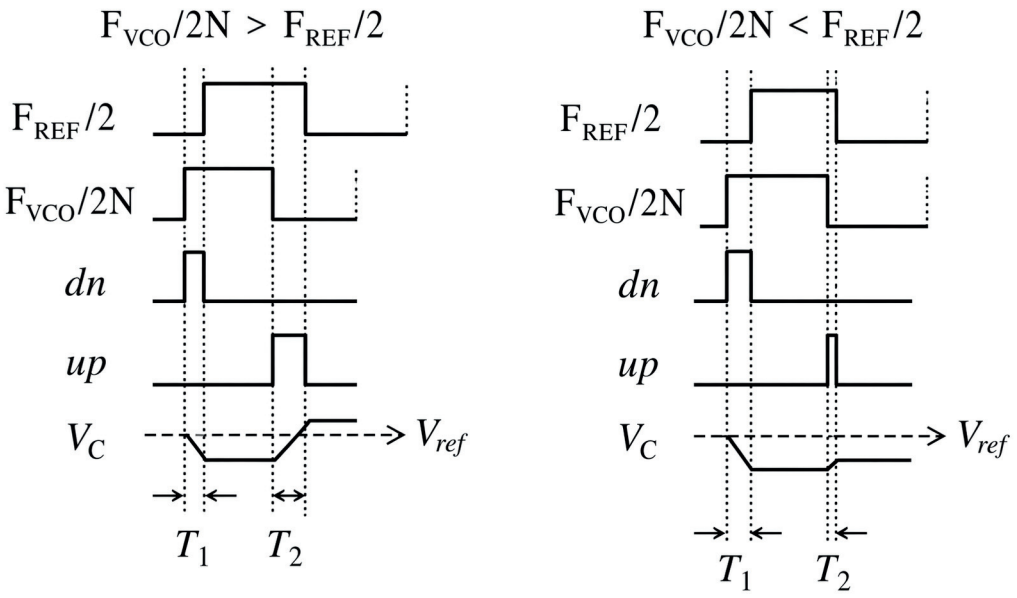

Figure 3.19: Operation timing diagram of the relative measurement

3.5.2. Proposed AFC Architecture

To reduce the AFC time, an improved TVC-based O-AFC technique is presented in [18]. No counters or extra clock circuits are used in the proposed AFC. Relying on a simple digital operable divide-by-3 (O-Div3) circuit and the reusing of reference frequency, the cycle of AFC can be realized within three reference periods. Synchronously, a new search algorithm is proposed for the optimized DCCA code without frequency error. Except the last step, the binary search algorithm is adopted in the proposed technique [18].

The AFC implementation is shown in Fig. 3.20. The loop here is the auxiliary FLL loop that we have discussed in the previous sections. The AFC takes inputs from the reference and the divided VCO output.

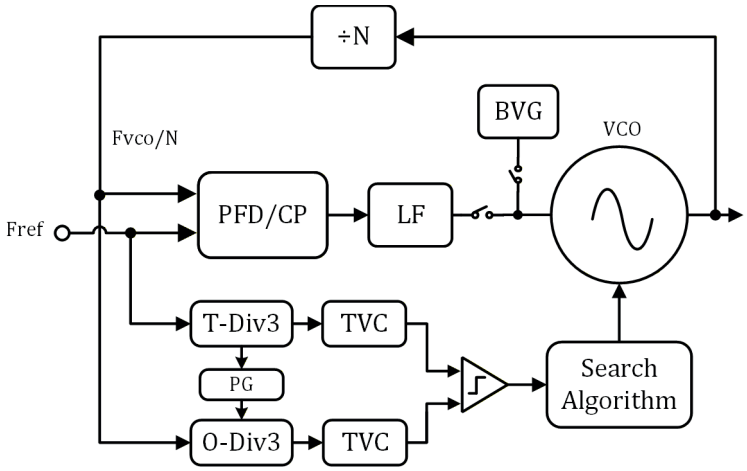

Figure 3.20: Block diagram of the proposed AFC

While traditional dividers (such as T-Div2 or T-Div3) can generate pulse widths proportional to signal periods, they suffer from the initial phase difference between the reference and the divided VCO signal. To eliminate this phase uncertainty, an O-Div3 circuit is employed, as depicted in Figure 3.21. By applying a narrow preset pulse to the DFFs, their initial states (Q1, Q2) are strictly forced to '00'. This initialization guarantees that the high-level phase of $F_{\text{div}}/3$ always starts deterministically with the arriving rising edge of F_{div}, enabling accurate time-domain sampling.

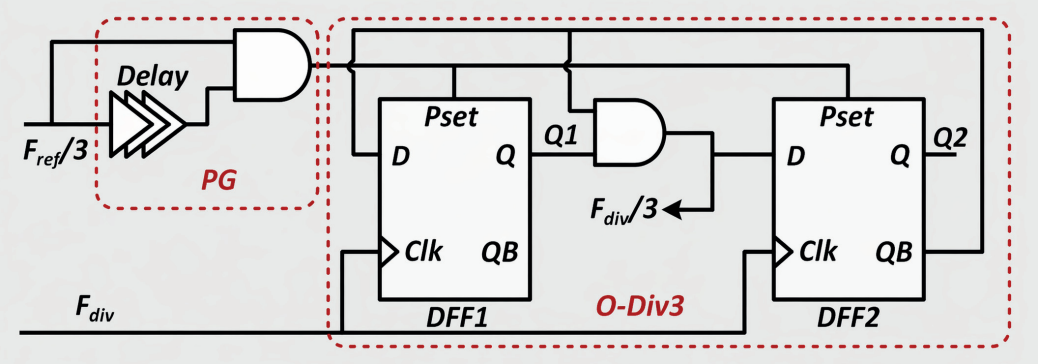

Figure 3.21: Implementation of O-Div3 circuit [18]

The timing diagrams corresponding to the initial states of Q1 and Q2 set to '10', '11', and '00' are illustrated below in Fig. 3.22, Fig. 3.23, and Fig. 3.24. As observed, only the '00' initial state ensures that the high-level phase of $F_{\text{div}}/3$ starts deterministically with the arriving rising edge of F_{div}.

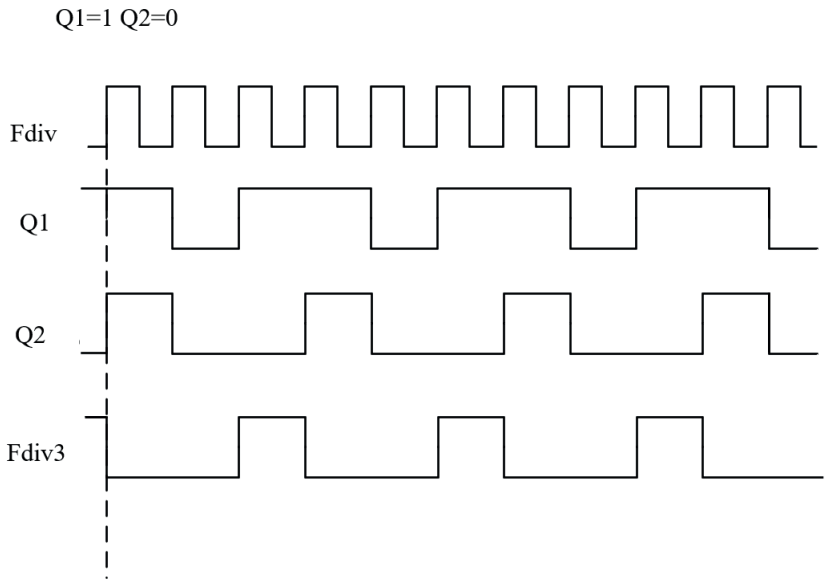

Figure 3.22: Q1Q2='10'

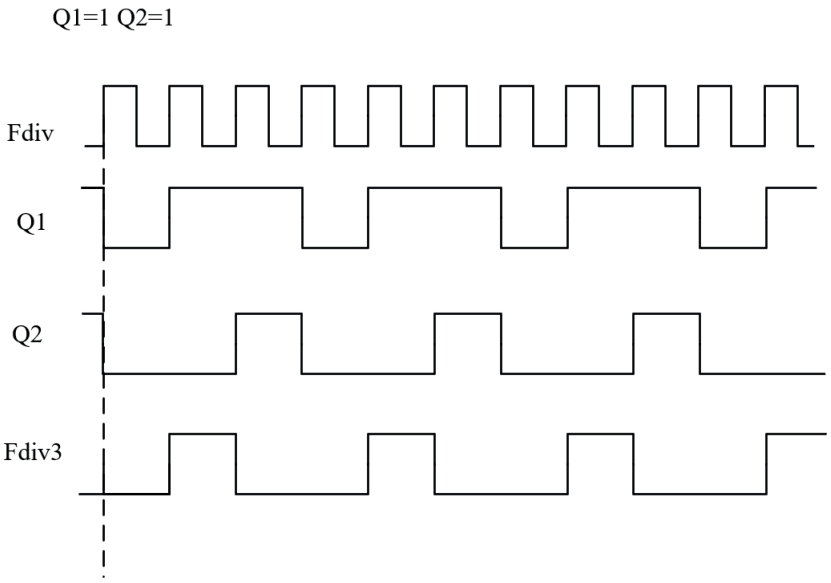

Figure 3.23: Q1Q2='11'

Here, $T_{\text{ref}} = 1/F_{\text{ref}}$ denotes the period of the reference clock, and $T_{\text{div}} = 1/F_{\text{div}}$ denotes the period of the divided VCO signal.

During the sampling phase, the high-level duration of $F_{\text{ref}}/3$, which corresponds to one period of the reference clock (T_{ref}), is converted into a reference voltage (V_{ref}) by charging the capacitor C_{ref} in the TVC. Concurrently, the pulse generator (PG) presets the O-Div3 circuit. This presetting operation ensures that the rising edge of $F_{\text{div}}/3$ is aligned with the rising edge of F_{div}. Subsequently, the high-level duration of $F_{\text{div}}/3$, which exactly corresponds to one period of the divided VCO signal (T_{div}), is converted into the voltage V_{div} across capacitor C_{div}. Once sampling is complete, a comparator evaluates V_{ref} and V_{div} to determine the appropriate discrete frequency band (DCCA code). Finally, the capacitors are discharged, readying the system for the next cycle. An AFC operation diagram is as shown in Fig. 3.25

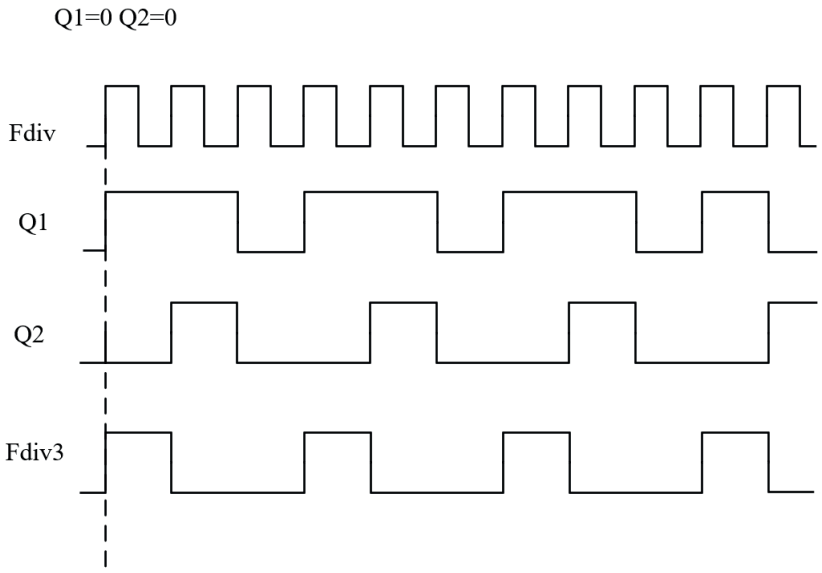

Figure 3.24: Q1Q2=’00’

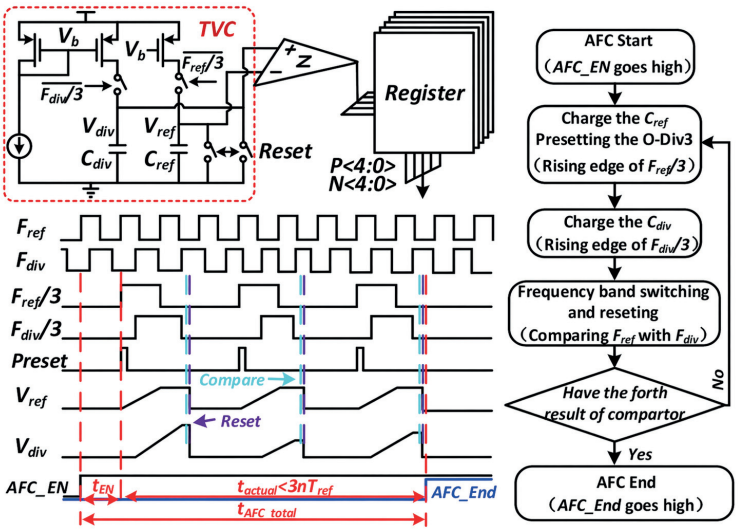

Figure 3.25: Timing diagram and flowchart of the proposed AFC. [18]

The presetting mechanism is crucial for ensuring temporal correctness, as analyzed in Figure 3.26. A complete AFC operation requires three reference periods: the first two are dedicated to accurate sampling, while the third acts as a buffer time for frequency band switching. This third period deliberately avoids sampling a corrupted waveform that contains mixed frequencies from two different bands. Consider the worst-case scenario where the rising edge of F_{div} aligns perfectly with the preset signal. In this case, the initial condition $Q_1Q_2 = 00$ cannot be guaranteed. Therefore, the $F_{\text{div}}/3$ signal reaches a high value only at the next rising edge of F_{div}. This entire procedure takes two periods of F_{div} ($2T_{\text{div}}$). Consequently, to ensure proper operation and to account for this worst case, the reference period must satisfy the following timing constraint:

$$T_{\text{ref}} > \frac{t_{\text{pset}} + 2T_{\text{div}} + t_{\text{comp}}}{3} \tag{57}$$

where t_{pset} and t_{comp} are the delays for presetting and comparing, respectively.

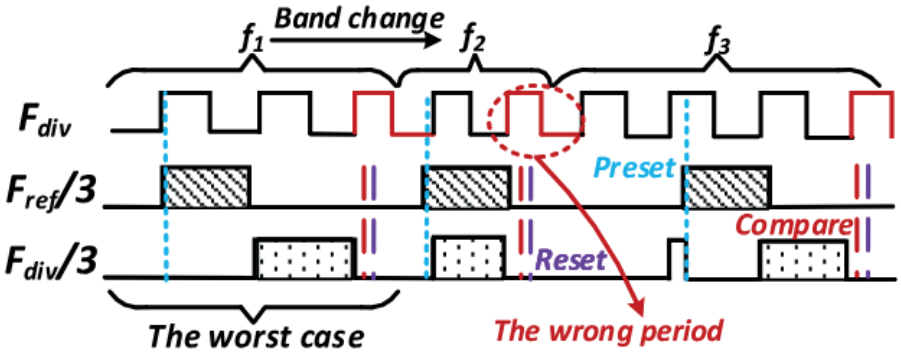

Figure 3.26: Waveform of the worst case for the proposed AFC. [18]

We must also consider the condition where T_{div} reaches its longest period. In other words, we need to evaluate how low F_{div} can be while still guaranteeing that the AFC algorithm manages to push the VCO output to the highest sub-band. Assuming an initial calibration frequency of f_{ini} and a maximum VCO frequency of f_{max}, with the division ration N fixed,

we have:

$$\frac{f_{\text{ini}}}{f_{\text{div,worst}}} = \frac{f_{\text{max}}}{f_{\text{ref}}} = N \tag{58}$$

Therefore, the longest possible period for T_{div} is formulated as:

$$T_{\text{div,worst}} = \frac{f_{\text{max}} \cdot T_{\text{ref}}}{f_{\text{ini}}} \tag{59}$$

Ignoring the minor delays in (57), this imposes a frequency tuning boundary of $f_{\text{max}} < 1.5 f_{\text{ini}}$. If this boundary is violated, a simple DFF-based detector triggers the DCCA code to jump to a higher frequency band, seamlessly resolving the overlap issue.

The search algorithm for the AFC is a new binary-like search algorithm without considering frequency error, unlike the traditional O-AFC techniques. Typically, the tuning voltage V_{tune} is set to $V_{\text{DD}}/2$, and the frequency error is evaluated by a binary search algorithm to determine the optimal DCCA code in the O-AFC. However, if a conventional binary search algorithm is applied to the proposed O-AFC, a sufficient frequency margin will be difficult to provide as [17] [18].

Figure 3.27 illustrates the principle of the proposed search algorithm. The digital control code is configured such that a higher DCCA value corresponds to a lower VCO frequency sub-band. This specific arrangement is deliberately adopted to align with the frequency tuning mechanism of the current-starved VCO, which will be detailed in the following section. Assume a simple equation:

$$f_{m,V_{\text{L}}} \approx f_{m+1,V_{\text{H}}} \tag{60}$$

where m represents the decimal value of the DCCA code, and $f_{m,V_{\text{L}}}$ denotes the VCO oscillating frequency when $V_{\text{tune}} = V_{\text{L}}$ under the m-th frequency band. This formula serves as the "safety net" of the entire algorithm. It ensures that adjacent frequency bands are connected without any gaps. Regardless of where the target frequency lies, it will always be bounded by two corresponding curves. Unlike the conventional approach of fixing V_{tune} to $V_{\text{DD}}/2$, the lower-bound voltage V_{L} is set by a bandgap voltage generator (BVG). When $F_{\text{ref}} > F_{\text{div}}$, the current and all higher frequency bands can be directly discarded. Otherwise, the current and higher frequency bands are selected. Based on this logic, a traditional binary search

algorithm can be utilized in the initial steps, while an extra calibration period is added to determine the final optimal DCCA code.

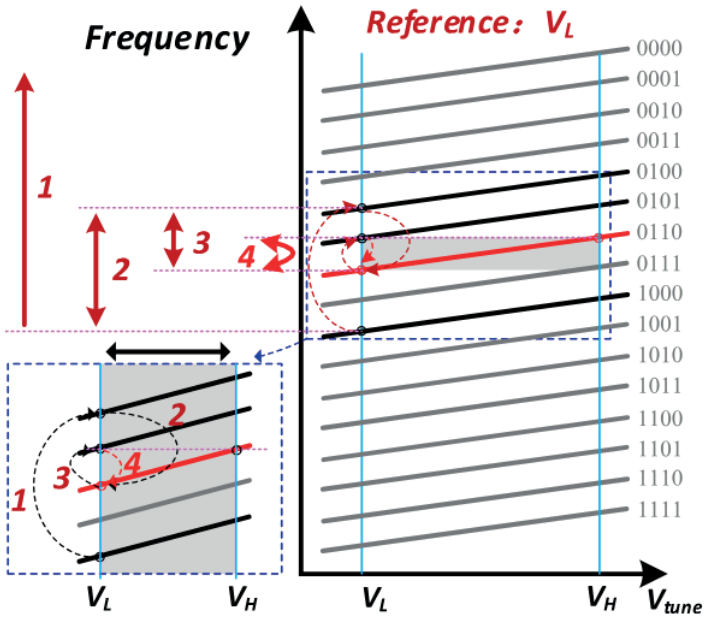

Figure 3.27: Search algorithm of the proposed O-AFC. [18]

We adopt an example from [18], assuming a 5 digit DCCA code. The block diagram is shown in Fig. 3.28. At the beginning of the algorithm, the DCCA code is initialized to "10000", and the binary search is applied for the first three calibration cycles. If the comparator output $OUTP$ is 1, the frequency band is switched upward; otherwise, it is switched downward. Hence, the switching mechanism is identical to a traditional binary search for the first three cycles. In the fourth step, an adaptive frequency band search is employed to find the optimal DCCA code between the two adjacent frequency bands. If $OUTP$ is 1, the frequency band remains unchanged; otherwise, the band is switched downward.

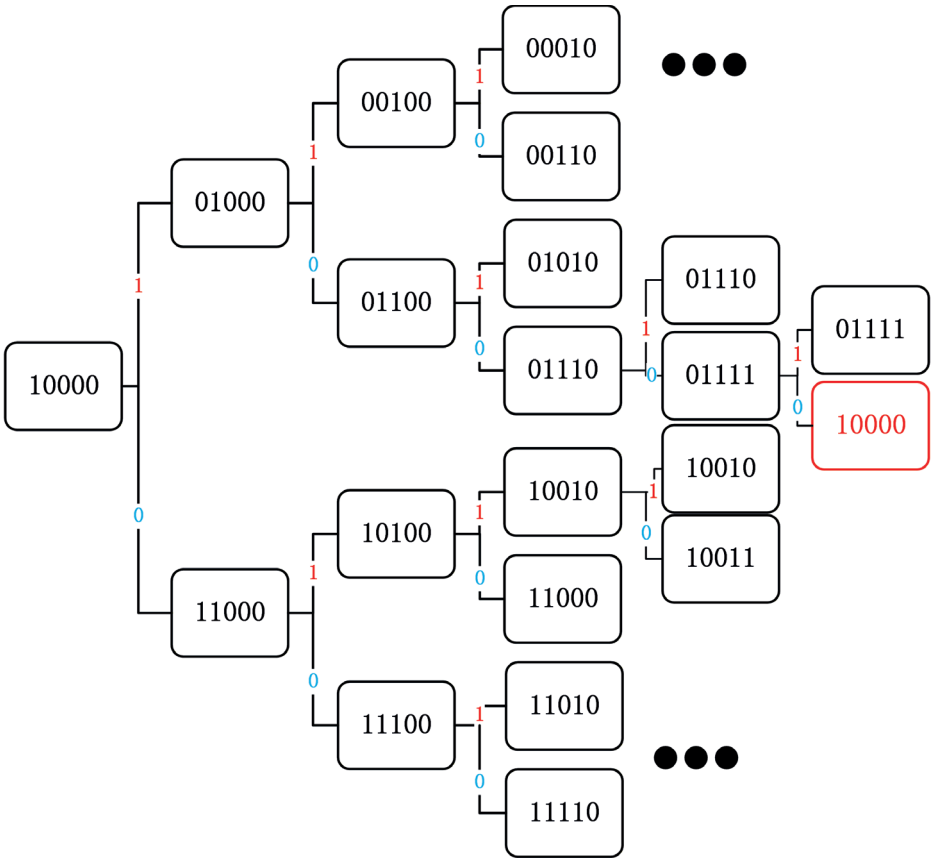

Figure 3.28: Switching scheme of the proposed O-AFC.

In the final stage of the frequency calibration algorithm, implementing a "+1" tuning step using conventional binary addition (e.g., code transition from "0111" to "1000") requires complex adder logic and causes simultaneous switching of multiple capacitor cells, leading to severe transient glitches. This situation is illustrated in the last step of the transition diagram in Fig. 3.28, where '01111' is added to '10000'. To deal with this issue in a practical way, the "+1" operation is mapped to its physical meaning: adding one LSB control cell to the VCO frequency control unit. A redundant LSB cell (dummy LSB) is placed in parallel with the main control array. During a "+1" operation, the main control code remains unchanged, and only the dummy LSB is activated, achieving an equivalent increment in total current

without carry-induced switching. Since the LSB cell is minimal, the parasitic impact when it is off is negligible in terms of phase noise. Therefore, this method trades a small analog area overhead for significant simplification of digital control logic and improved system stability.

4. CIRCUIT DESIGN

In the preceding sections, the theoretical foundations and system-level analysis of the proposed dual-path SSPLL have been comprehensively discussed. Building upon this system-level framework, this section shifts the focus to the actual physical implementation of the PLL. The detailed transistor-level circuit design of each core building block will be presented module by module, including the SSPD, the SSCP, the current-starved Ring VCO, and the digital AFC circuits, etc.

4.1. SSPD

The circuit design of the SSPD is shown in Fig. 4.1.

As for SSPD, it is basically a Sample & Hold circuit. Since there are inevitable non-idealities of switches that have to be used in a Sample & Hold circuit, it is necessary to connect an isolation buffer between the SSPD and the VCO to prevent charge sharing at least.

The isolated differential VCO output signal is fed back into the negative and positive inputs of the sampler, where we use a transmission gate as the switch. We only need a single S&H stage since the pulser acts like the second stage, as mentioned in the previous section.

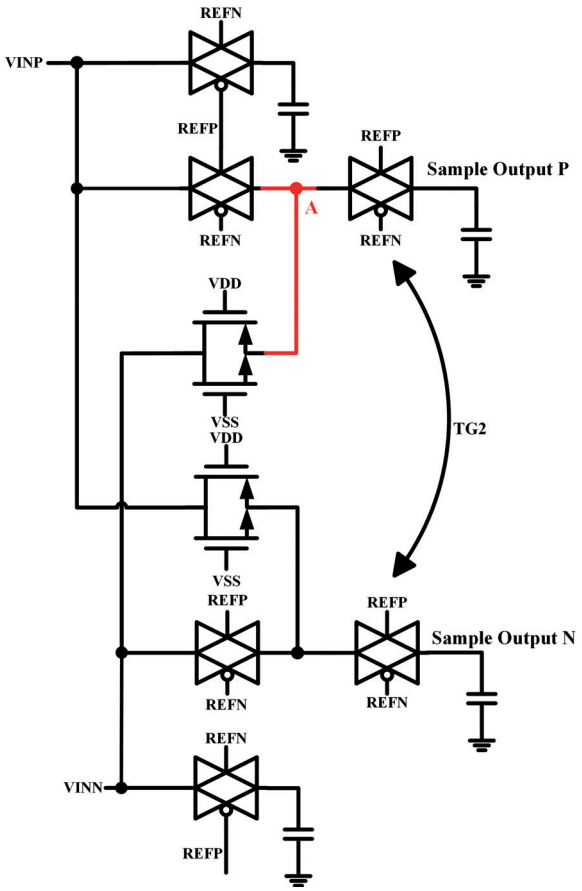

Figure 4.1: Circuit design of the SSPD

However, degeneration of linearity has to be considered as well, for different input voltage levels cause different voltage drops across the transistors, meaning different operation speed for the switches. This kind of error will cause mismatches between charging/discharging current from SSCP, harming the phase noise performance of the PLL. One way to attenuate this effect is to use larger W/L transistors in the switch, to minimize the speed variation for different input voltage levels. At the same time, it is important to make sure that the switches exhibit negligible charge sharing effect with increasing W/L, making a good trade-off between these two effects.

During the hold mode, parasitic AC coupling of the signal still occurs across the off-state switches and must be compensated. To mitigate this effect, another two transmission gates that are designed to be always cut off during the operation can be connected between the input node and the middle node between the two switches at the sampler output path, to provide an extra path for charge to flow. Since the input signal is differential with a phase shift of 180°, the injected AC currents at the intermediate node perfectly cancel each other out. Consequently, the AC coupling from the two inputs is effectively eliminated. Thus, the voltage at node A can be regarded as clean, enabling the second sampler to produce an accurate output.

As for the output of the VCO, it is ideal that the loading to it is always the same, for different loadings cause frequency changes, harming noise/spur performance of the PLL via FM modulation. So, there are two dummy paths in this SSPD to ensure the same loading seen by the VCO during the whole operation.

4.2. SSCP

The schematic of the SSCP is shown below in Fig. 4.2.

The differentially sampled voltages, INN and INP, are fed into a PMOS differential pair for voltage-to-current (V2I) conversion. The converted current from the INN branch is fed into a current mirror to act as the DN current source at the output. Conversely, the INP signal is first converted into an N-type current source and then transformed into a P-type current source through a current mirror chain. This P-type current is subsequently copied to serve as the UP current.

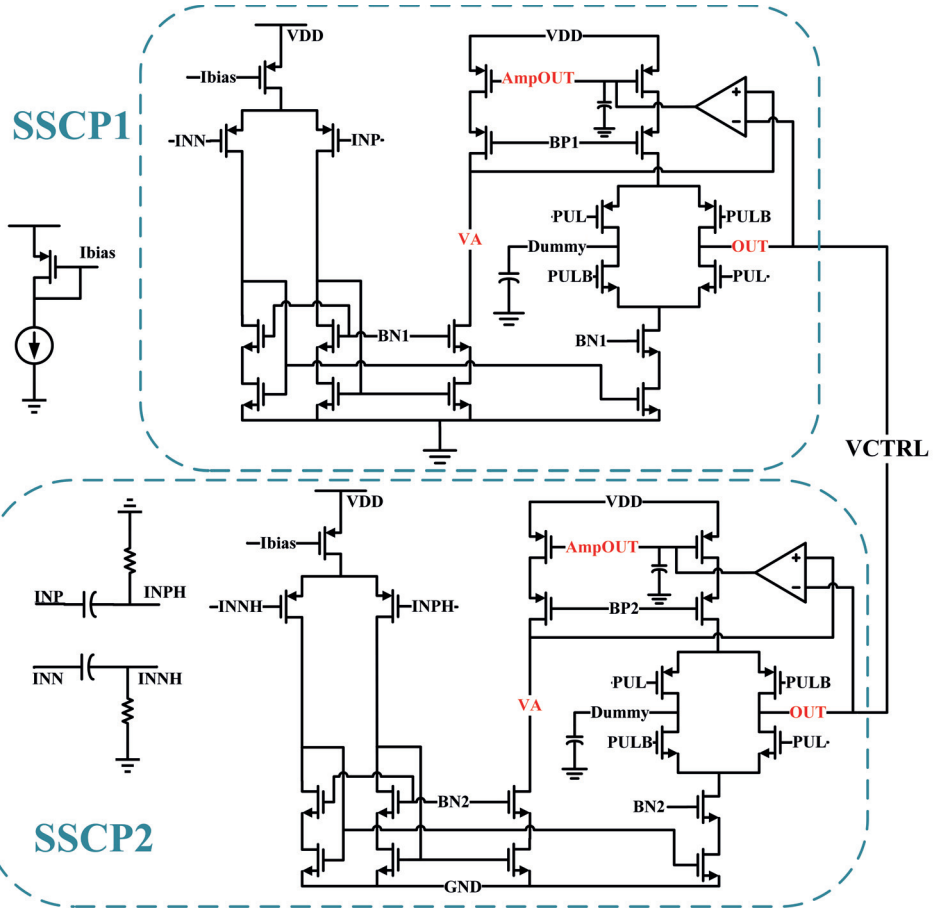

Figure 4.2: Circuit design of the SSCP

For the dual-path architecture, the second path includes a high-pass filter (HPF). The INN and INP signals are first high-pass filtered before being fed into the PMOS pair of SSCP2. The subsequent operations are identical to those in SSCP1.

An error amplifier is utilized to track the variations on the control line to ensure that the transistors in both current mirror paths share the same drain-source voltage. Furthermore, transistors with larger channel lengths are selected to further suppress the current mismatch.

Note that two capacitors are employed in this CP design. The first capacitor is connected between the dummy output node and the ground. Since during the regular operation of

SSCP, pulse signal generated from the pulser is usually very narrow compared with reference clock, normally occupying only 10-20 percent pulse width of the period clock, which means its dummy path conducts most of the time. And when transitions between dummy path and main path happen, the capacitor connected between the dummy output node and the ground absorbs some charge injected from the channel of the dummy switches, alleviating some ripple problems on the control voltage line. Also, this dummy structure alleviates clock feed-through effect, because dummy path and output path are controlled by opposite clock, and this is why the source of the PMOS switches only experience very limited clock feed-through effect, same for the NMOS switches.

Here we don't need an Op Amp to ensure same node voltage for the dummy node and the output node. The CP adopted a current-steering topology, where I_{UP} and I_{DN} are either connected to LF or dumped to a capacitor C_{dump}. Ideally, there is no charge sharing if the voltages on d1 and d2 are kept constant during switching, i.e., if we can set $V_{\mathrm{LF}} = V_{\mathrm{dump}}$. In a conventional CP, this requires a unity-gain buffer. Here, this is achieved for free as explained below. In steady state, the net charge into the LF and C_{dump} should be both zero. Since I_{UP} and I_{DN} have equal on-time in both "connected to LF" and "dumped to C_{dump}" cases, they must also have equal amplitude in both cases. This condition is met only if $V_{\mathrm{LF}} = V_{\mathrm{dump}}$, where the finite current source output impedance is actually the equalizing mechanism. [19]

The second capacitor is placed at the output node of the error amplifier, which is also the gate of the PMOS current mirrors. Since one of the input terminals of the amplifier is directly connected to the main voltage control line, any high-frequency AC ripples present on V_{ctrl} can easily couple into the amplifier. If left unaddressed, these fluctuations would induce corresponding ripples at the amplifier output, directly disturbing the gate bias of the current mirrors. To eliminate this noise propagation, the added capacitor acts as a low-pass filter to absorb the AC components. It ensures that a clean and steady bias voltage is continuously provided to the current mirrors, thereby guaranteeing the proper and stable operation of the CP.

4.2.1. Pulser

Another important block to mention in the SSCP is the pulser. As mentioned before, the pulser is used to control the PD/CP gain to a value that is not unnecessarily large. Also, the pulser is also used as the second sample and hold stage.

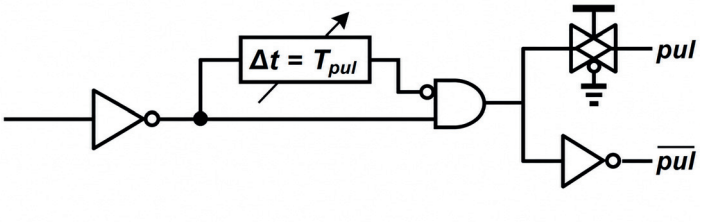

Figure 4.3: Circuit design of the Pulser

The circuit design of the pulser is shown in Fig. 4.3. Consider the falling edge of the reference clock. The lower path is initially at logic ”0” and switches to ”1” immediately, while the upper path is initially at logic ”1”. As a result, the AND gate outputs a ”1”. This output remains high for a duration equal to the pulse width T_{pul}. When the upper path transitions to ”0”, the AND gate output returns to ”0”, marking the end of the pulse.

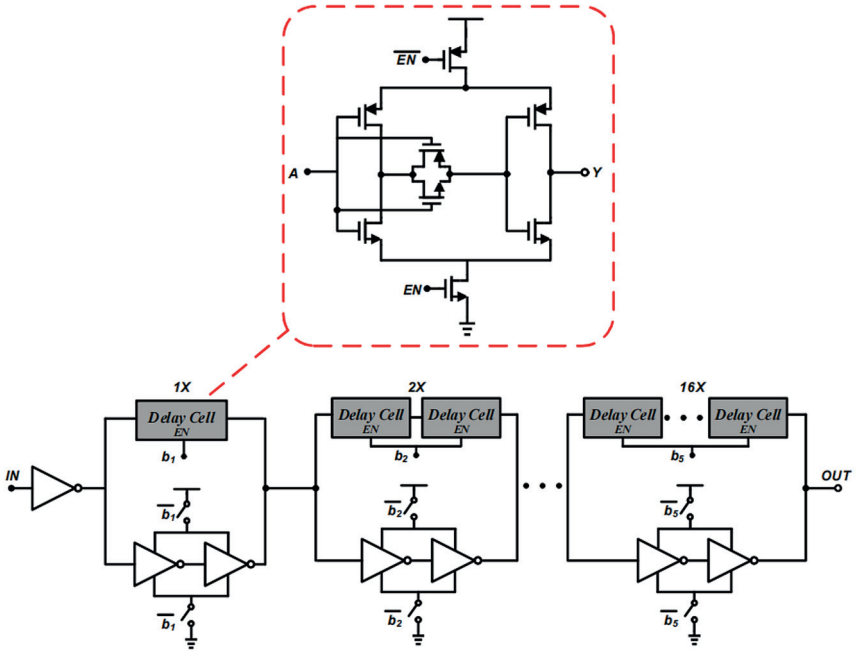

Figure 4.4: Circuit design of the Pulser control unit

The pulser is programmable to optimize loop performance. As can be seen in Fig. 4.4, the pulse width is controlled by digital code b1 to b5. By inserting a transmission gate dynamically controlled by the input signal between the stages, this circuit exhibits the high-impedance characteristics of the transistors during the switching transient to apply strong RC filtering and damping to the signal. Consequently, it achieves a much larger delay compared to conventional cascaded inverters without significantly increasing the chip area.

4.3. VCO

A ring VCO is used in this design rather than an LC VCO, because of the strong suppression effect of VCO noise from the wide bandwidth of the PLL, and wide frequency tunning range requirement. The circuit design of the ring VCO is as shown in Fig. 4.5.

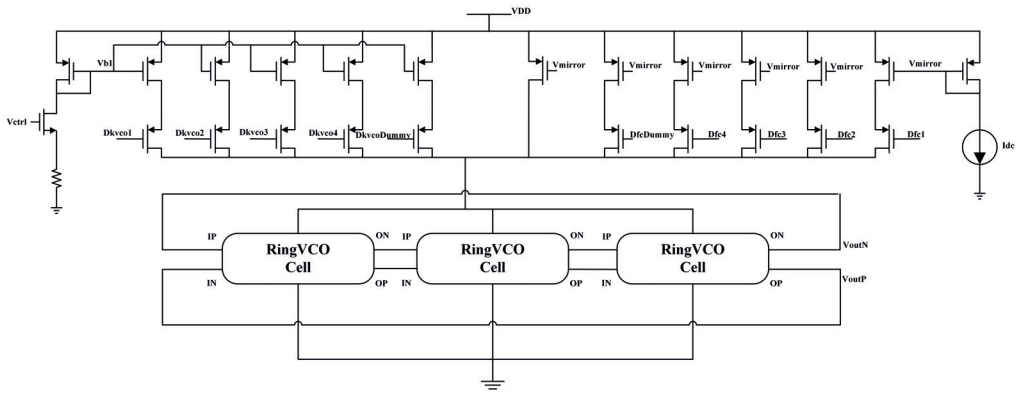

Figure 4.5: Circuit design of the current-starved VCO

In order to achieve wide tuning range from 2GHz to 4GHz, there are four bits of coarse tuning (D_{fc}) and four bits of K_{VCO} gain trimming switches to achieve approximately the same VCO gain for all of the course tuning bands (D_{KVCO}), since large K_{VCO} gain deviations harm the phase noise performance and stability of the loop, and the four bits of trimming provide margin for PVT variations. A look up table (LUT) is used to match the DKVCO bits to the corresponding Dfc bits. The LUT matching is shown on the next page in Table I:

Table II: LUT of Dfc and Dkvco

Dfc	**Dkvco**	**Dfc**	**Dkvco**
0000	0000	1000	0100
0001	0000	1001	0100
0010	0001	1010	0101
0011	0001	1011	0101
0100	0010	1100	0110
0101	0010	1101	0110
0110	0011	1110	0110
0111	0011	1111	0111

Also, there are two dummy current mirrors for AFC operation (it will be explained later in the AFC section).

Regarding the noise analysis of the VCO, the current mirrors translate their low-frequency flicker noise and broadband white noise into the $1/f^3$ and $1/f^2$ phase noise regions at the VCO

output via frequency modulation. To minimize these noise contributions, the dimensions of the current mirror transistors must be carefully sized. Specifically, the power spectral density (PSD) of the thermal current noise is proportional to the transconductance g_m:

$$S_{i,th} = 4kT\gamma g_m \tag{61}$$

where γ is the channel noise factor (approximately 2/3 for long-channel devices). A smaller aspect ratio (W/L) reduces g_m, thereby effectively suppressing the thermal noise. Simultaneously, the flicker noise PSD is inversely proportional to the transistor's gate area ($W \times L$):

$$S_{i,1/f}(f) = \frac{K_f g_m^2}{C_{ox} W L f} \tag{62}$$

where K_f is the flicker noise coefficient and C_{ox} is the oxide capacitance. Therefore, selecting transistors with a small W/L ratio but a large overall $W \times L$ area optimally minimizes both the white and flicker noise components.

For the voltage-to-current (V2I) converter, a source degeneration topology is employed, providing two significant advantages. First, it linearizes the V-to-I conversion. The effective transconductance G_m becomes largely independent of V_{ctrl}, transitioning the output current relationship from a non-linear square-law behavior to a linear one. This ensures a highly linear VCO tuning gain (K_{VCO}). Second, the source degeneration resistor R significantly reduces the overall current noise. The equivalent noise PSD is improved from the standalone transistor noise to a degenerated form:

$$S_{i,\text{V2I}} \approx 4kT\left(\gamma G_m + \frac{1}{R}\right) \tag{63}$$

where $G_m \approx g_m/(1 + g_m R)$. As shown in the equation above, by choosing a sufficiently large R, G_m is heavily degenerated, leading to a much lower injected noise current. The V2I converter circuit is shown in Fig. 4.6.

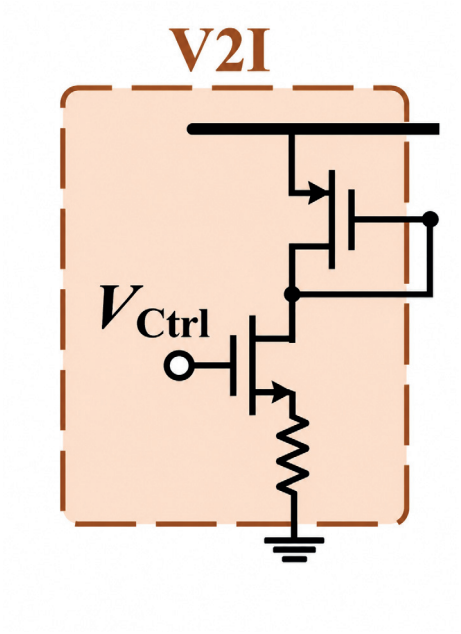

Figure 4.6: V2I converter in VCO. [20]

The core of the ring VCO is based on a 3-stage differential current-controlled oscillator (CCO). The block diagram and circuit design is shown in Fig. 4.7 and Fig. 4.8 respectively.

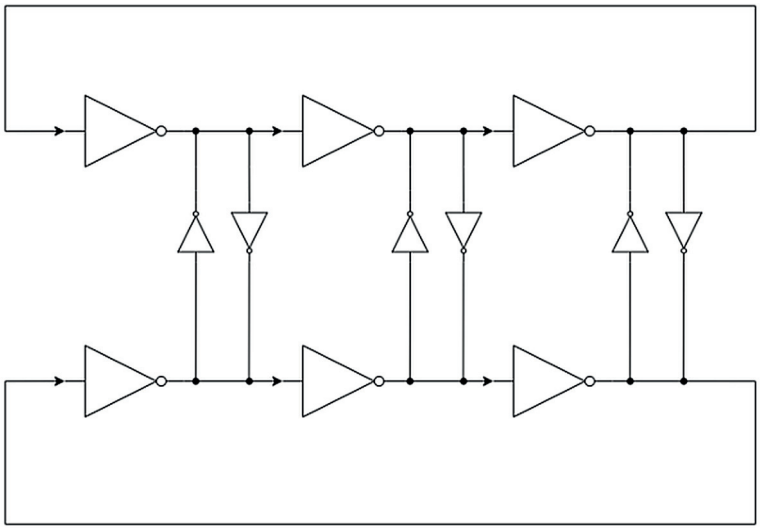

Figure 4.7: Block diagram of the ring VCO

To enhance the switching performance, auxiliary cross-coupled inverters are embedded within each delay stage to provide positive feedback. When a differential transition occurs, this latching mechanism actively pulls the complementary nodes to their respective logic levels. Consequently, the transition time is shortened, leading to a much steeper zero-crossing slope (higher slew rate). By sharpening the transition edges, the time window during which the oscillator is sensitive to noise injections is significantly reduced, thereby yielding an improved jitter and phase noise performance.

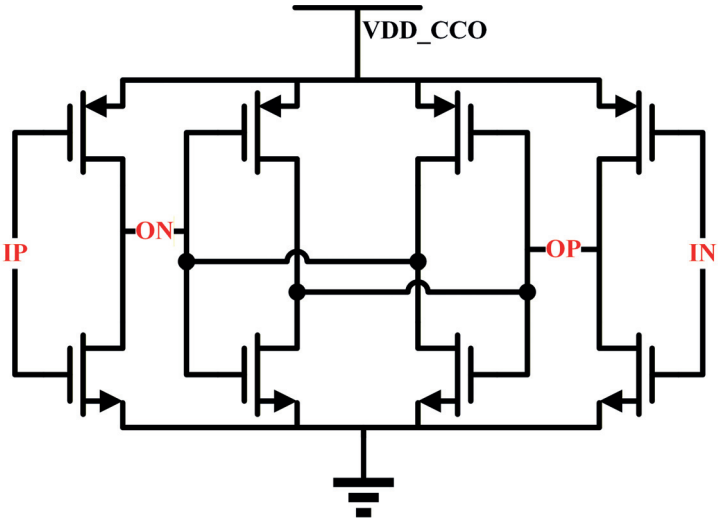

Figure 4.8: Circuit design of the CCO cell

4.4. PFD with DZ

The PFD with Deadzone is shown in Fig. 4.9. Note that the delay for Q1D and Q2D determines the width of deadzone for the PFD, simply because delay line equivalently puts a requirement for the pulse widths of the inputs of the AND gate not to be too narrow, or it will end up with zero output.

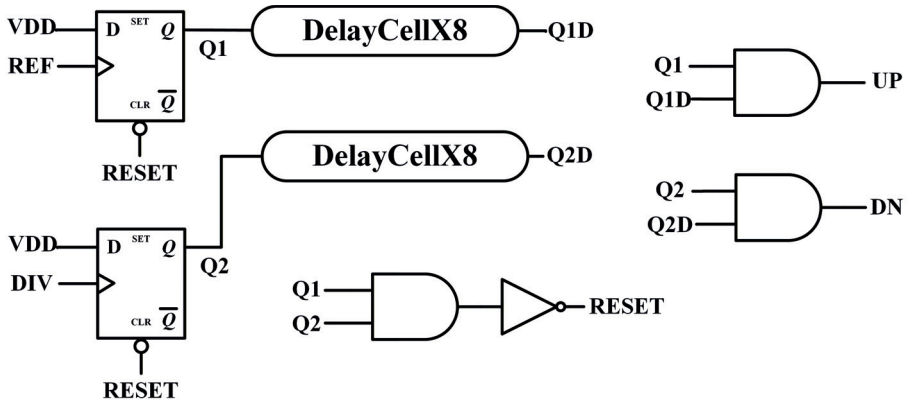

Figure 4.9: Circuit design of the PFD with DZ

4.5. CP in FLL

Since the operating principle of the CP in the FLL used here is essentially identical to that of the SSCP described earlier, a detailed discussion is omitted to avoid redundancy.

4.6. Divider

Figure 4.10 illustrates the architecture of the proposed pulse-swallow (PS) frequency divider. Since conventional static CMOS digital counters cannot directly process the multi-gigahertz signals generated by the VCO, a high-speed dual-modulus prescaler (e.g., a divide-by-5/6 prescaler) is required as the first stage. This prescaler steps down the high-frequency signal to a much safer and lower range, enabling the subsequent digital counters to operate reliably.

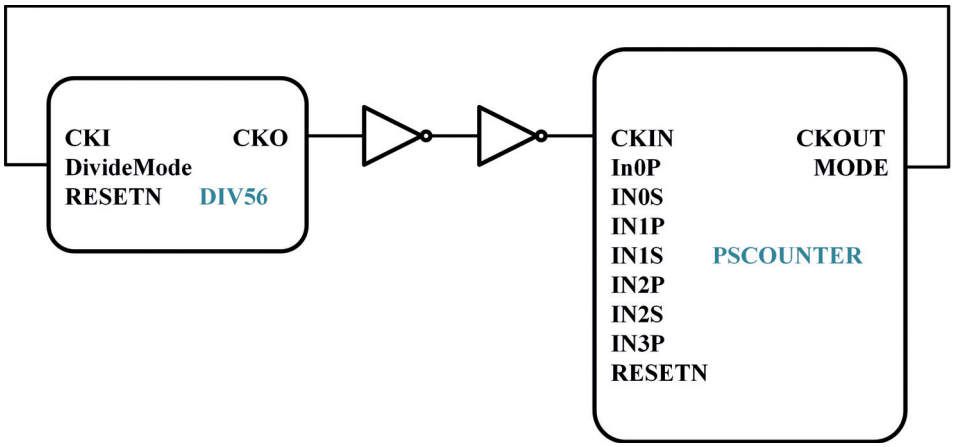

Figure 4.10: Block Diagram of the Prescaler

The overall division operation is executed through a systematic counting cycle. At the beginning of the cycle, the dual-modulus prescaler processes the incoming VCO signal using its divide-by-$(N+1)$ mode (i.e., divide-by-6, where $N = 5$). The prescaled output clock is then simultaneously fed to both the Program (P) counter and the Swallow (S) counter, which begin counting the rising edges concurrently. By design, the preset value of the P counter is strictly larger than that of the S counter ($P > S$).

Once the S counter reaches its programmed value, it triggers a modulus control signal that is fed back to the prescaler. This control signal forces the prescaler to switch its operating mode from divide-by-6 to divide-by-5 (divide-by-N). Subsequently, the P counter continues to count the remaining $(P - S)$ cycles of the newly prescaled clock. When the P counter finishes its counting task, a complete division cycle concludes, and an output pulse is generated and delivered to the following output buffers.

Based on this operation mechanism, the total frequency division ratio D_{total} provided by the PS divider can be formulated as:

$$D_{\text{total}} = (N+1)S + N(P-S) = N \cdot P + S \tag{64}$$

4.7. ISO-Buffer

This is the isolation buffer used in this design as shown in Fig. 4.11. self-biased inverters are used here to stabilize the output common mode voltage level, making it independent of the common mode voltage level of the VCO output, also biasing both PMOS/NMOS transistors at the region with high transconductance to ensure proper amplitude of its output, for its amplitude is important for the bandwidth of the SSPLL.

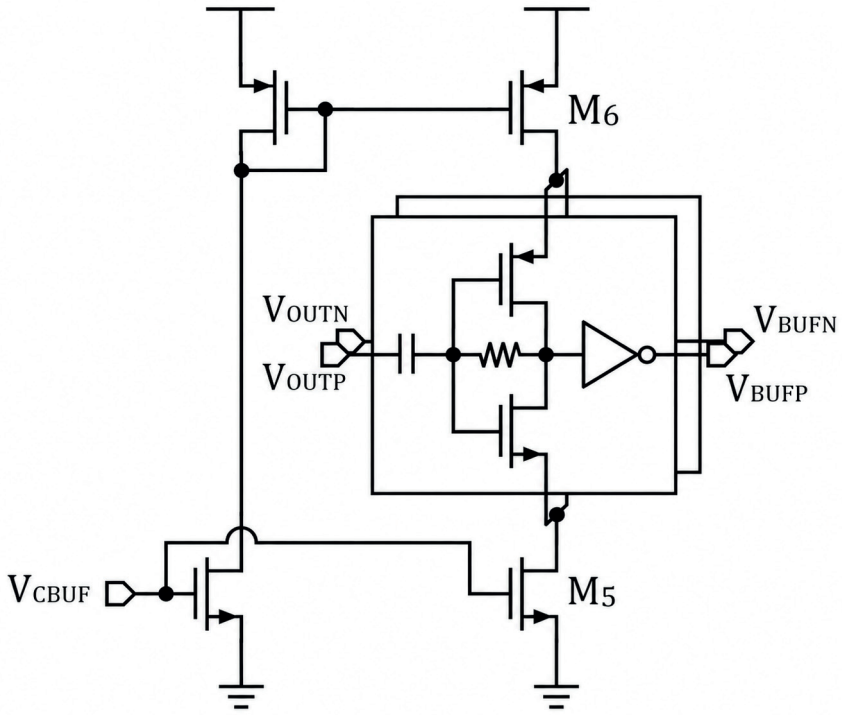

Figure 4.11: Differential ISO-Buffer Design. [21]

4.8. T-DIV3 & O-DIV3

In the proposed AFC design, a T-Div3 circuit is employed in the reference path to generate $F_{\text{ref}}/3$, which defines the sampling window for the reference TVC. Meanwhile, an O-Div3 is utilized in the feedback path to generate $F_{\text{div}}/3$. Unlike a conventional divider, the O-Div3

incorporates a preset operation. This operation initializes the internal DFFs, ensuring that the high-level phase of $F_{\text{div}}/3$ deterministically aligns with the correct rising edge of F_{div}.

Specifically, the O-Div3 functions as a state machine composed of DFFs, and its output phase heavily relies on the initial states of these flip-flops. Without a preset mechanism, the divider may start from a random state, causing the high-level pulse of $F_{\text{div}}/3$ to appear at unpredictable F_{div} cycles. By applying the preset signal, the DFFs are forced into a predefined state prior to sampling. Consequently, the subsequent F_{div} edge triggers a strictly predictable $F_{\text{div}}/3$ waveform. Thus, the preset operation does not alter the phase of the high-frequency signal (F_{div}) itself; instead, it dictates the starting state of the divider to synchronize the phase of the divided output. The O-Div3 circuit is implemented as such in Fig. 3.21. A delay and an AND gate are used to generate a pulse that is aligned with the rising edge of $F_{\text{ref}}/3$, with a pulse width equal to the delay. The output of the AND gate is fed to the reset inputs of the DFFs, forcing the outputs to Q1Q2 = "00".

As a result, the feedback TVC accurately samples the intended VCO period, preventing measurement errors caused by initial phase uncertainties or frequency-band switching transients. In summary, the T-Div3 provides a stable reference timing window and the O-Div3 generates a phase-aligned feedback sampling pulse. This allows the AFC to complete one calibration cycle within exactly three reference periods, saving power, space, and time consumed.

The circuit design of the T-Div3 is shown in Fig. 4.12

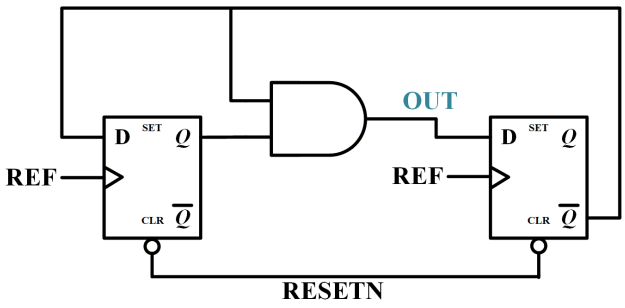

Figure 4.12: Circuit design of the TDiv-3

Figure 4.13 illustrates the schematic of the TVC employed in the AFC module. The core mechanism relies on converting the pulse widths of $F_{\text{div}}/3$ and $F_{\text{ref}}/3$ into proportional charging durations for the sampling capacitors. After the charging phase, the resulting steady-state voltage levels are delivered to the subsequent comparator to guide the frequency search algorithm. At the end of each calibration cycle, the charge stored on these capacitors must be completely reset. To guarantee the precision of the sampled voltages, non-ideal effects from the sampling switches must be strictly minimized, as any residual charge would severely corrupt the final output voltage level of the TVC.

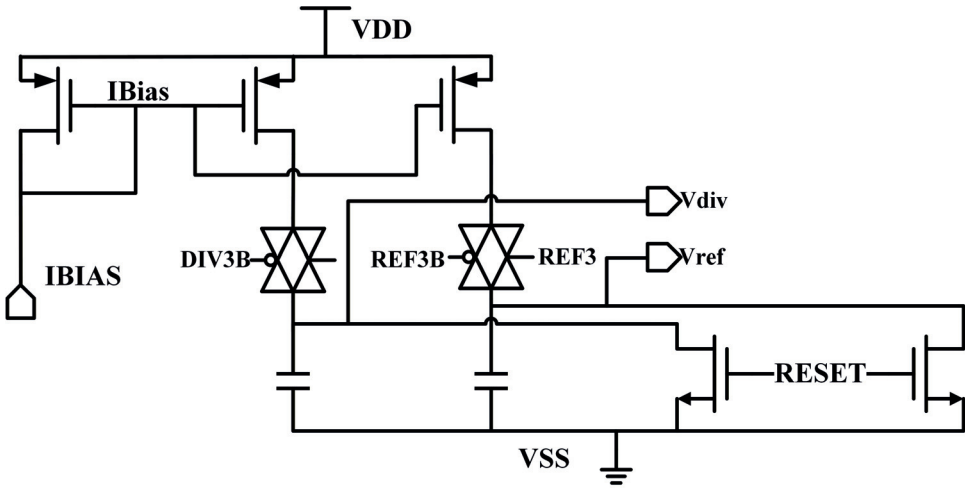

Figure 4.13: Circuit Design of the TVC

To address these non-idealities, a charge-compensated switch topology is utilized in the TVC, as shown in Figure 4.14. Alongside the main transmission gate, two NMOS and two PMOS dummy transistors are introduced. These dummy devices are driven by inverted control signals to actively absorb the channel charge injected during the turn-off transitions of the main switches, thereby effectively mitigating charge injection and clock feedthrough issues.

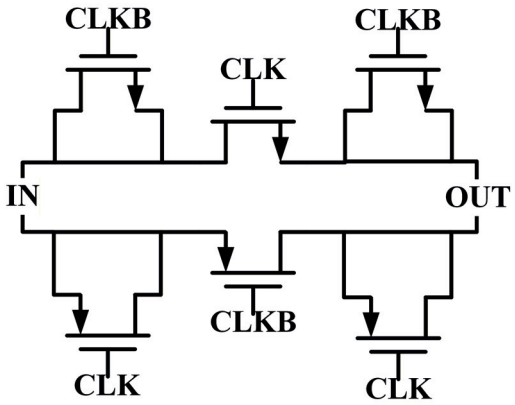

Figure 4.14: Circuit Design of the switch in TVC

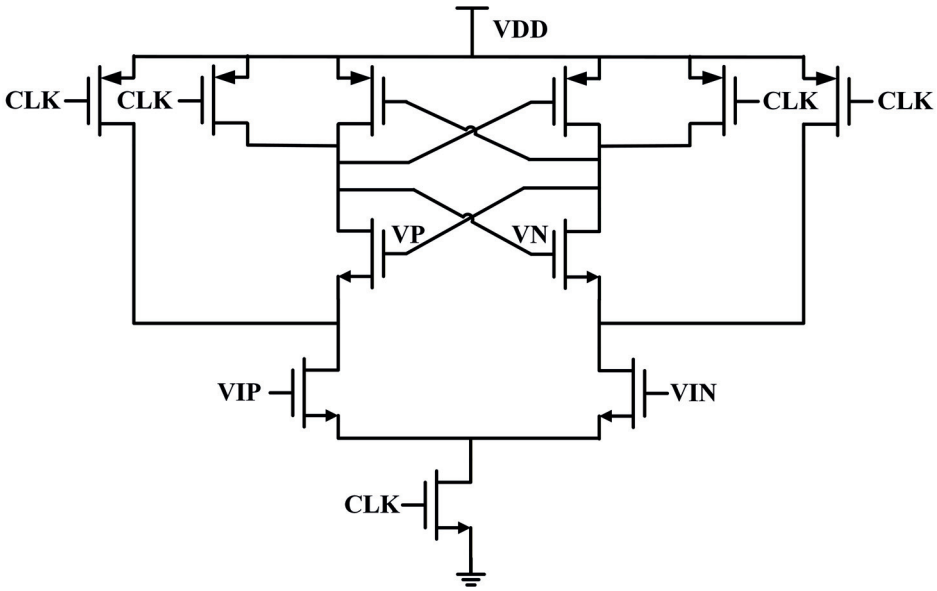

Figure 4.15: Circuit Design of the Comparator

Following the TVC, a dynamic regenerative comparator is implemented to evaluate the voltage difference, as depicted in Figure 4.15. Compared to conventional static comparators, this dynamic architecture offers superior speed and negligible static power consumption.

During the reset phase, the internal nodes are pre-charged to the supply voltage. Once the comparison phase begins, the input differential pair translates the sampled voltage error into a minute voltage difference at the internal nodes. A positive-feedback cross-coupled latch then rapidly amplifies this small difference into full rail-to-rail digital logic levels. This topology is highly advantageous for the AFC loop due to its zero static current, high-speed operation, and robust full-swing outputs.

5. SIMULATION RESULTS

Following the theoretical analysis and circuit-level implementation detailed in the previous sections, this section presents the simulation results to verify the overall performance of the proposed dual-path SSPLL. The entire PLL system is designed and simulated using Cadence Virtuoso in a standard 65-nm CMOS process. To comprehensively evaluate the proposed architecture, the following subsections will successively present the behaviors of the main blocks, the phase noise, jitter performance, and the power consumption across the operating frequency range.

5.1. SSCP

As can be seen in Fig. 5.1, the charging and discharging currents match each other well across the charge pump output voltage from 0.15 volts to 1.05 volts, ensuring stability of the PLL across a wide frequency tuning range.

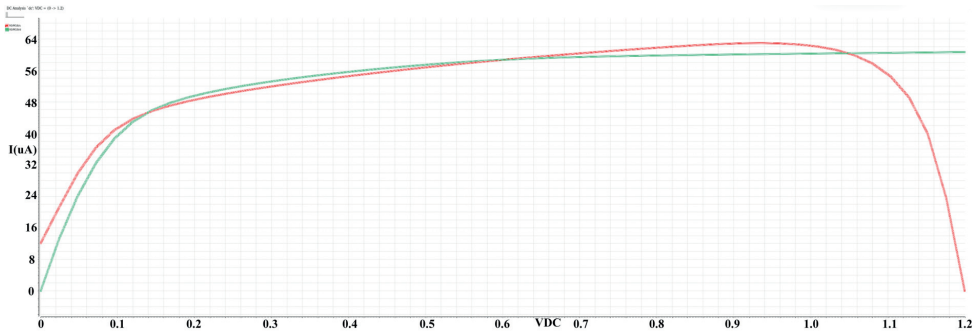

Figure 5.1: SSCP DC current

5.2. Pulser

The transient simulation of the pulser is shown in Fig. 5.2. The red waveform represents the reference-related sampling clock, while the green waveform is the generated pulser signal. As can be seen from the waveform, the pulser generates a narrow rail-to-rail pulse once in every reference period. The pulse is deliberately arranged to be non-overlapping with the sampling clock, so that the SSCP is only activated after the sampling operation is completed.

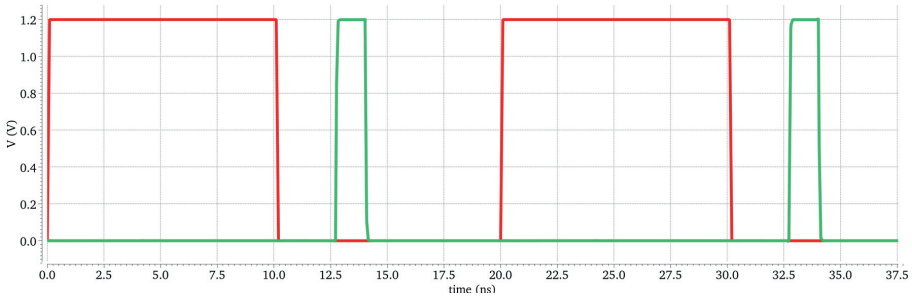

Figure 5.2: Transient simulation of the reference clock and the generated pulser signal

A zoomed waveform of the pulser operation in the PLL loop is shown in Fig. 5.3. The orange waveform is the pulser signal, and the red waveform shows the sampled output of the SSPD. Small periodic ripples can still be observed around the pulser active region. These ripples are mainly caused by the finite charge injection, clock feedthrough, and current mismatch during the switching operation of the SSCP.

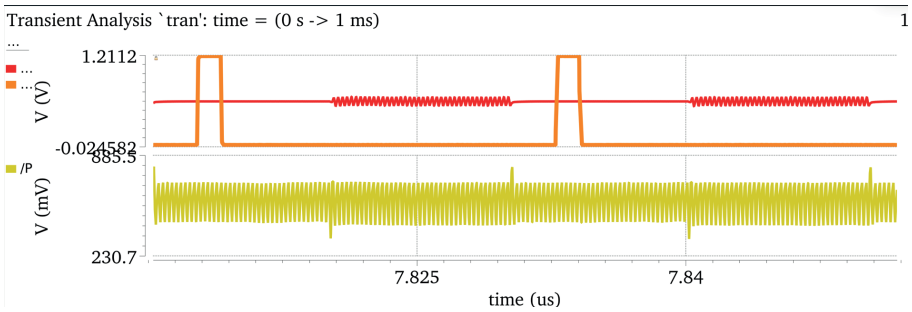

Figure 5.3: Zoomed transient waveform of the pulser operation in the PLL loop

5.3. VCO

Figure 5.4 shows the frequency sub-bands of the VCO. The total tuning range covers from approximately 1.6 GHz to 4.2 GHz. Adjacent sub-bands overlap with each other, providing sufficient margin for process, voltage, and temperature (PVT) variations.

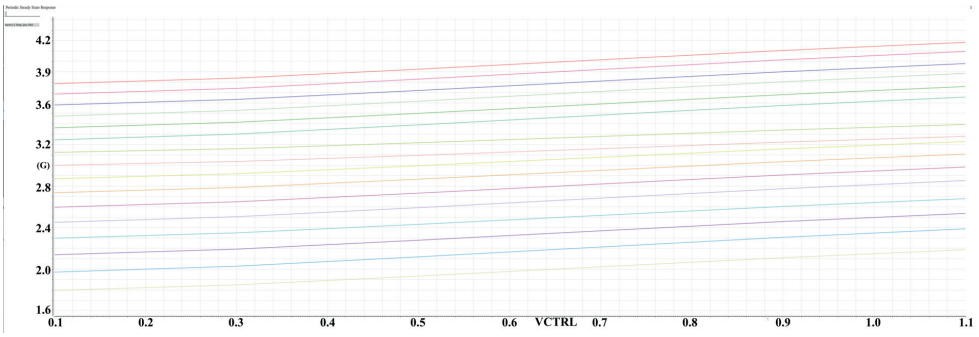

Figure 5.4: VCO sub-bands

Figure 5.5 illustrates the simulated phase noise of the free-running VCO. By sweeping the digital control code (D_{fc}), the VCO operates across the 2 GHz to 4 GHz range. The phase noise curves exhibit similar characteristics across these different frequencies. At a 10-MHz offset, the phase noise varies from -110.6 dBc/Hz to -113.5 dBc/Hz.

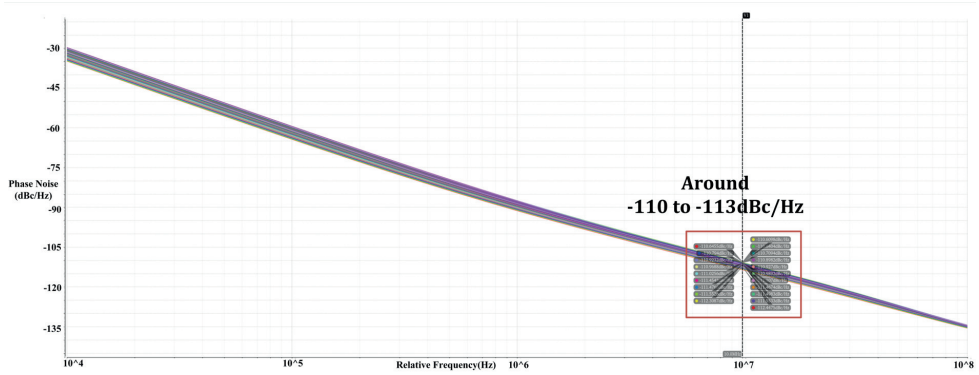

Figure 5.5: Phase noise performance of free-running VCO

5.4. PFD with DZ in FLL

The PFD-CP characteristic of the PFD with DZ in FLL is shown in Fig. 5.6

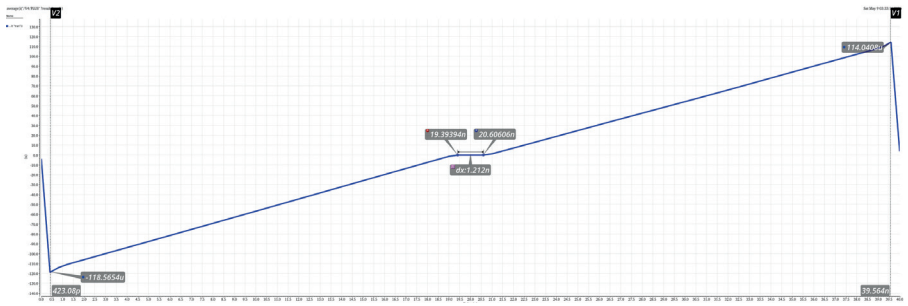

Figure 5.6: PFD/CP characteristic with DZ

5.5. Divider

Shown below in Fig. 5.7 is the transient simulation of the divider. The input source is set to have a frequency of 7 GHz, to have some margin for post-layout parasitic effects, which typically degrade the maximum operating frequency of digital circuits. Due to the cascaded nature of the prescaler, the input signal is first fed into a Divide-by-5/6 divider, and then into the counters, as discussed in the previous section. Therefore, dividing a signal of 7 GHz by a ratio of 40 would be the most critical case for the divider.

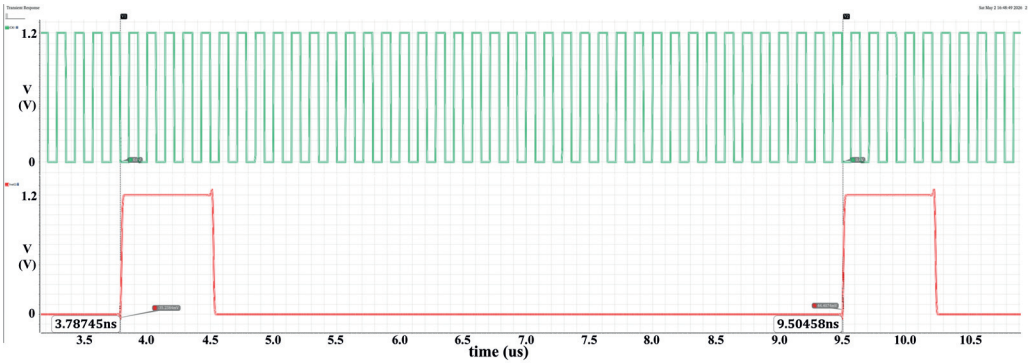

Figure 5.7: Transient simulation of the divider

Figure 5.8 shows the transient simulation of the SSPLL operating at a 2.05 GHz output frequency with the AFC algorithm activated. The locking process can be divided into 3 stages. First, from 0 to about 387 ns, the digital AFC operates to select the most suitable VCO sub-band. Second, from 387 ns to approximately 2.4 μs, the analog FLL is activated to perform coarse tuning, which rapidly reduces the frequency error and pulls the VCO output frequency toward its target.

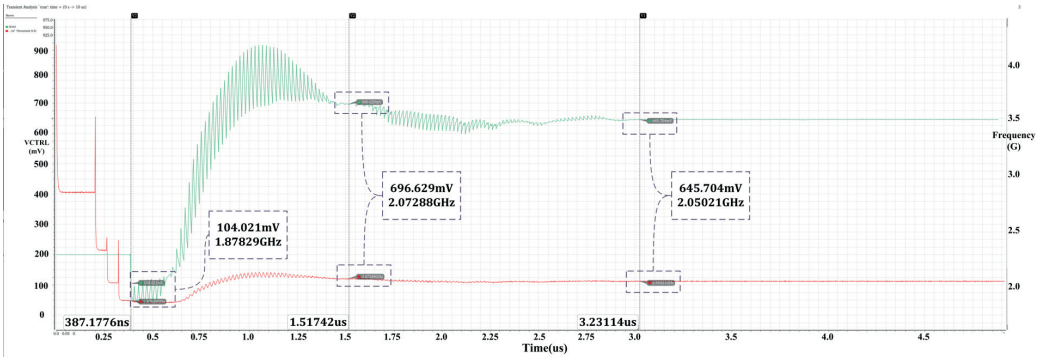

Figure 5.8: Transient simulation of the loop with AFC activated

During this FLL coarse tuning period, a dynamic handover occurs between the FLL and the core sub-sampling loop. Initially, the FLL pulls the frequency aggressively, bringing the system into the dead zone from the phase-lag side. This temporarily enables the core SSPLL at around 1.5 μs. However, due to the limited phase detection range of the core loop, the frequency error induced by the FLL with the dead-zone still remains, keeping accumulating the phase error for the system, which causes the FLL to fall out of its dead-zone.The DN signal of the FLL is then reactivated to pull the frequency back down. After this transient overshoot is resolved at around 2.4 μs, the FLL enters the dead-zone permanently. From this point until approximately 3 μs, the core sub-sampling loop takes full control, eventually achieving phase locked state.

The simulation of AFC_done signal proves the working region of the AFC algorithm, as shown in Fig. 5.9. At 387ns, AFC_done is "1", meaning the AFC has done its job.

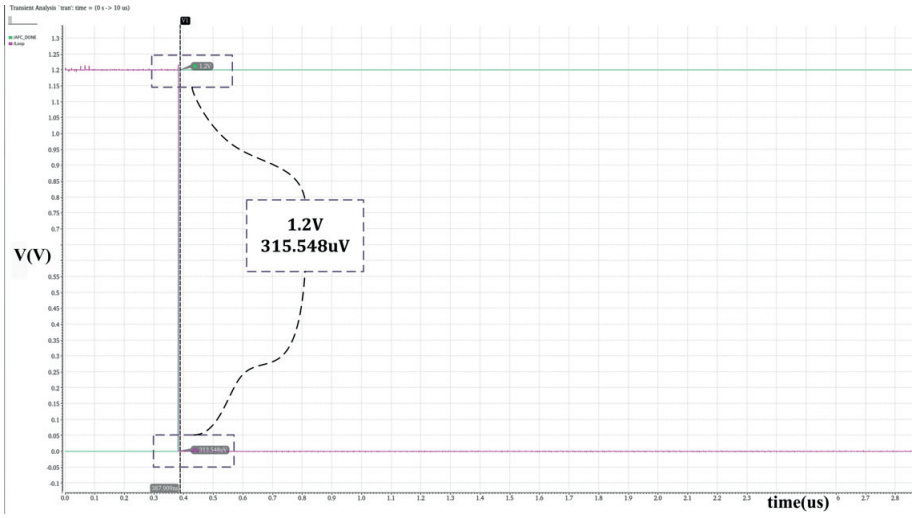

Figure 5.9: AFC_done

The UP and DN signal shown below in Fig. 5.10 also support the above working procedures.

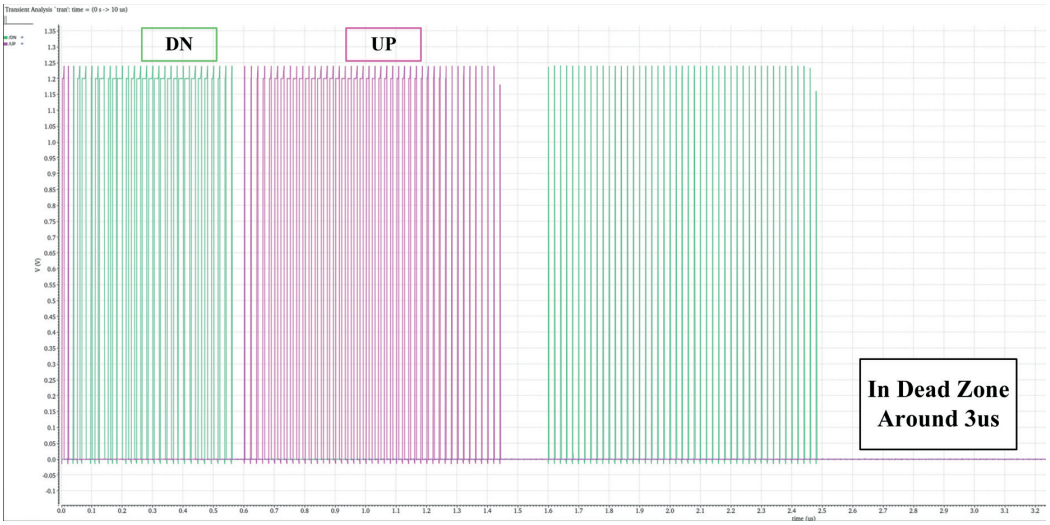

Figure 5.10: UP and DN in CP of FLL

Figure5.11 shows the feedback frequency. As can be seen in the waveform, the PLL is settled at about 3us, with the AFC activated.

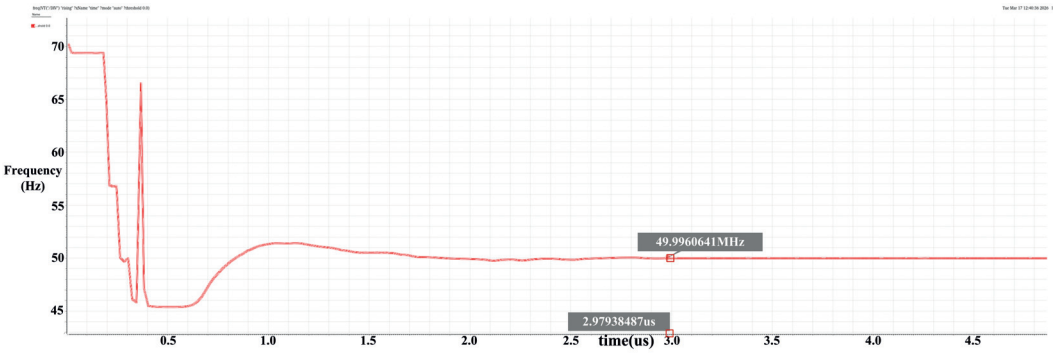

Figure 5.11: Transient behavior of the divided output signal

5.7. Loop Behavior

As for the bandwidth of the PLL. It can be seen in Fig. 5.12, the loop bandwidth is around 5MHz. The phase noise of the PLL is -111.357 dBc/Hz @10 MHz offset.

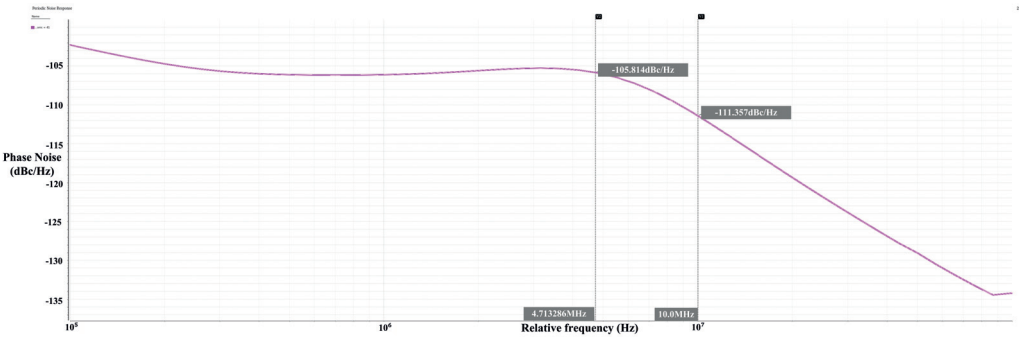

Figure 5.12: Loop Bandwidth of the SSPLL operating at 2.05GHz

The jitter performance in seconds can be calculated by integrating the phase noise spec-

trum across a specific offset frequency range. The RMS absolute jitter is formulated as:

$$J_{rms} = \frac{1}{2\pi f_c}\sqrt{\int_{f_1}^{f_2} \mathcal{L}(f)\, df} \tag{65}$$

where f_c is the output carrier frequency, $\mathcal{L}(f)$ represents the single-sided phase noise power spectral density in linear scale, and f_1 and f_2 define the lower and upper limits of the integration bandwidth, respectively. Here the upper limit is 100 MHz and the lower limit is 100 kHz. Since it is hard to make the PSS simulation converge when operating at 4 GHz(because of larger division ratio), we use the phase noise plot when operating at 2.05 GHz. The RMS jitter is then 1.24 ps.

5.8. MATLAB-Based 4-GHz Transient-Noise Post-Processing

Since the PSS and Pnoise simulation becomes difficult to converge when the PLL operates at 4 GHz, especially with a larger division ratio and a long locking transient, an alternative transient-noise post-processing method is adopted in this work. Instead of directly obtaining the phase-noise result from Pnoise simulation, the PLL output waveform is first simulated using transient noise analysis. The output waveform is then exported as a CSV file and processed in MATLAB.

In this post-processing, the PLL output is regarded as a 4-GHz square wave. Since the loop requires some time to complete the acquisition process, only the waveform after 6 μs is used for the FFT and phase-noise calculation. The rising edges of the output waveform are extracted to estimate the edge timing error, and the corresponding phase error is then used to calculate the phase-noise spectrum. Meanwhile, a uniform resampling and FFT operation are performed on the output waveform to observe the carrier-related spectrum and the spur components around the 4-GHz carrier.

It should be noted that this method is only used as an auxiliary verification for the 4-GHz operating condition. Due to the limitation of simulation time, hardware resources, and working environment, it is not practical to run a much longer and higher-resolution transient-noise simulation. Therefore, the following MATLAB-based result may not fully reflect the most accurate phase-noise and spur performance of the actual circuit. Nevertheless, it still

provides a useful reference for observing the noise and spur behavior when the PLL operates at the highest target frequency.

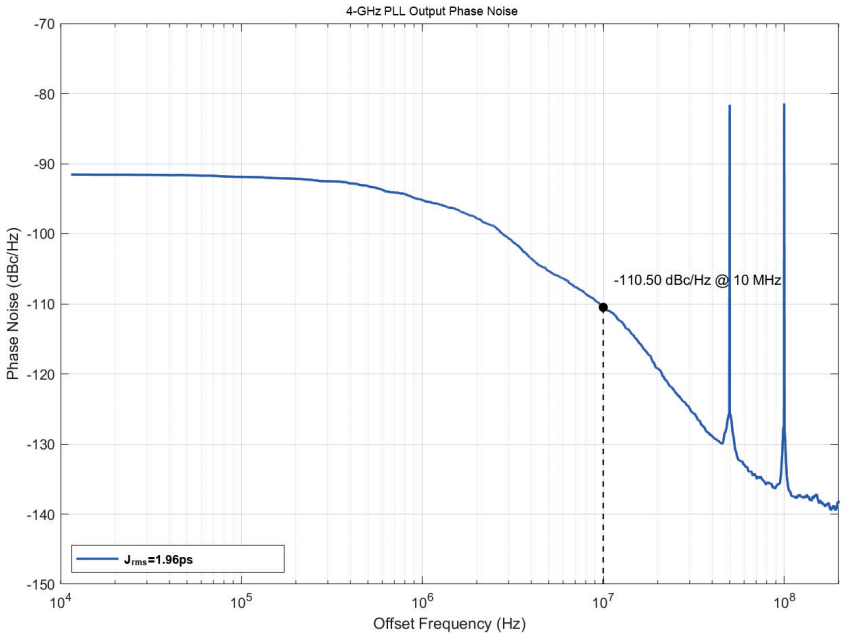

Figure 5.13: MATLAB post-processed phase-noise curve of the 4-GHz PLL output based on rising-edge timing error

As shown in Fig. 5.13, the phase noise is obtained from the timing variation of the rising edges after the PLL reaches the stable region. The phase noise is -110.5 dBc/Hz at 10 MHz. The integrated jitter estimated is 1.96ps

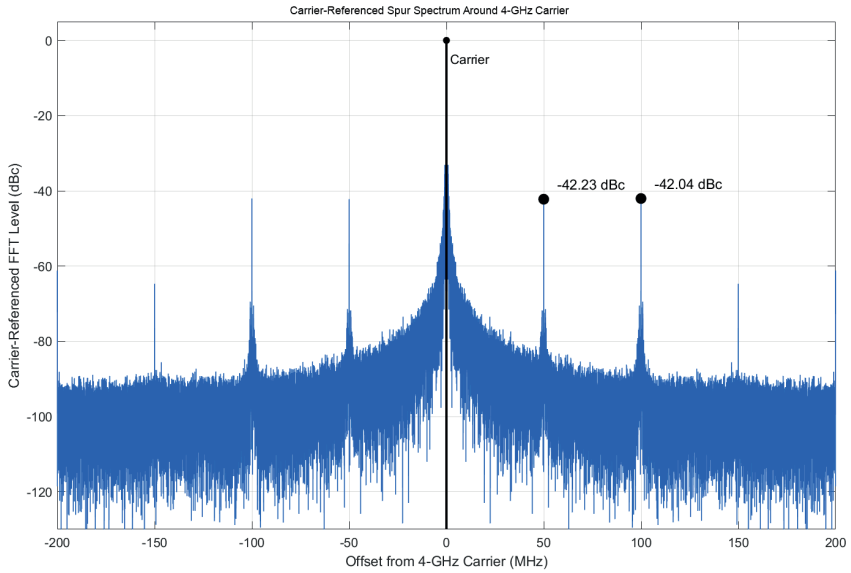

Figure 5.14: MATLAB post-processed FFT spectrum around the 4-GHz PLL output carrier

Figure 5.14 shows the FFT spectrum around the 4-GHz carrier. It can be seen that several discrete spur components appear at the offset frequencies related to the reference clock and its harmonics. The extracted reference-related spur levels are listed in Table III. In this simulation setup, the dominant reference-related spurs appear around 50 MHz and 100 MHz offset, with levels of approximately −42 dBc.

Table III: Reference-related spur levels from MATLAB FFT post-processing at 4 GHz

Harmonic	**Target Offset**	**Measured Offset**	**Spur Level**
1	50 MHz	49.999 MHz	−42.23 dBc
2	100 MHz	99.998 MHz	−42.04 dBc
3	150 MHz	150.002 MHz	−64.72 dBc
4	200 MHz	199.997 MHz	−61.20 dBc

The relatively high spur level at 4 GHz can be explained from two aspects. First, when the

operating frequency is increased, the bandwidth limitation of the feedback buffers becomes more critical. If the buffer bandwidth is not sufficient, the signal amplitude and slew rate at the SSPD is reduced. For the sub-sampling path, a smaller and slower waveform directly reduces the effective phase-detection gain of the SSPD. For the auxiliary frequency-acquisition path, the degraded feedback waveform also weakens the effective detection behavior of the PFD. As a result, the equivalent loop gain is reduced, making the loop more sensitive to the ripple on the control voltage.

Second, at the 4-GHz operating point, the PLL may lock with a certain static phase offset. In this case, the PFD in the auxiliary FLL may not fully stay inside the designed dead zone after locking. Therefore, the auxiliary loop can still generate periodic UP or DN pulses. These pulses introduce extra periodic current injection into the loop filter, producing ripple on the VCO control voltage. Since the ring VCO is sensitive to the control voltage variation, this ripple is translated into frequency modulation at the PLL output and finally appears as reference-related spurs in the output spectrum.

Therefore, the spur performance at 4 GHz is mainly limited by the high-frequency buffer bandwidth, the reduced effective phase-detection gain, and the residual activity of the auxiliary FLL. Further optimization can be achieved by increasing the bandwidth and driving capability of the feedback buffers, improving the dead-zone design of the auxiliary FLL, reducing the mismatch and charge injection of the charge pump paths, and further suppressing the ripple on the VCO control line.

5.9. Performance Summary and Comparison

Following the block-level and system-level simulation results presented above, the main target specifications and achieved performance of the proposed PLL are summarized in Table **??**. The target of this thesis is not only to achieve low jitter at a single frequency point, but also to maintain a wide tuning range with low power consumption. Therefore, the VCO tuning range, loop bandwidth, locking behavior, phase noise, integrated jitter, and power consumption are considered together.

Table IV: Key performance targets and simulated results of the proposed PLL

Parameter	**Target**	**Simulated Result**
RMS jitter	$<$ 1 ps, integrated from 100 kHz to 100 MHz	1.24 ps, integrated from 100 kHz to 100 MHz
Output frequency tuning range	2 GHz to 4 GHz	VCO sub-bands cover approximately 1.6 GHz to 4.2 GHz
Loop bandwidth	Around 5 MHz	Approximately 5 MHz at 2.05 GHz output frequency
Phase noise	< -110 dBc/Hz at 10-MHz offset	-111.357 dBc/Hz at 10-MHz offset
Power consumption	< 5 mW	6 mW at 2.05 GHz output frequency

As can be seen from Table IV, the simulated VCO tuning range is wider than the required 2 GHz to 4 GHz output frequency range. This provides extra margin for process, voltage, and temperature variations. The complete PLL simulation is mainly evaluated at 2.05 GHz because the PSS simulation becomes difficult to converge at higher operating frequencies with a larger division ratio. Nevertheless, the VCO tuning curves and block-level simulation results indicate that the proposed architecture is able to cover the desired operating range.

To further evaluate the proposed design, Table V compares this work with several previously reported PLLs and frequency synthesizers. Since different works use different architectures, frequency ranges, jitter integration bandwidths, and phase-noise offset frequencies, the comparison should not be interpreted as an absolutely fair ranking. Instead, it is used to show the relative position of this work in terms of power consumption, tuning range, jitter, and architecture complexity.

Table V: Performance comparison with prior works

Reference	**Process**	**Frequency**	**Power**	**Jitter**	**Phase Noise / Feature**	**FoM**
[3]	0.18 μm	2.21 GHz	7.56 mW	0.15 ps	-126 dBc/Hz @ 200 kHz	-247.7 dB
[9]	45 nm	2.4 GHz	4 mW	0.97 ps	-114 dBc/Hz @ 1 MHz	-234.1 dB
[7]	65 nm	2–2.8 GHz	5.86 mW	0.633 ps	-123.5 dBc/Hz @ 300 kHz	-236.3 dB
[4]	–	2 GHz	0.16 mW[a]	2.63 ps	6.5-dB maximum noise suppression @ 1.1 MHz	–
[21]	40 nm	5.3–5.9 GHz	1.8 mW	0.1965 ps	-119.9 dBc/Hz @ 1 MHz, referred to 5.6 GHz	-251.6 dB
This work	65 nm	2–4 GHz	6 mW	1.24 ps	-111.357 dBc/Hz @ 10 MHz	-230.35 dB

[a] Only the additional phase-noise-suppression path power is reported for this row.

Compared with the prior works, this work focuses on a wide output frequency range from 2 GHz to 4 GHz while keeping the power consumption at 6 mW. Although the absolute jitter FoM is not the best among the listed designs, the proposed architecture achieves a useful balance among wide tuning range, low power, ring-VCO integration, and fast digital-assisted locking. This is especially important because ring VCOs usually suffer from much worse phase noise than LC VCOs. By using the sub-sampling phase detector and the dual-path bandwidth-extension technique, the loop bandwidth can be increased to around 5 MHz, allowing the ring VCO phase noise to be suppressed more effectively.

The jitter figure-of-merit is calculated to provide a more direct comparison between different designs. In this thesis, the following commonly used jitter FoM is adopted:

$$\mathrm{FoM}_{\mathrm{jitter}} = 10\log_{10}\left[\left(\frac{\sigma_t}{1\ \mathrm{s}}\right)^2 \cdot \left(\frac{P_{\mathrm{DC}}}{1\ \mathrm{mW}}\right)\right] \tag{66}$$

where σ_t is the integrated RMS jitter and P_{DC} is the DC power consumption in mW. For the proposed PLL, the simulated RMS jitter is 1.24 ps and the total power consumption is 6 mW. Therefore,

$$\mathrm{FoM}_{\mathrm{jitter}} = 10\log_{10}\left[\left(\frac{1.24\times10^{-12}}{1}\right)^2\cdot 6\right] \tag{67}$$

$$= -230.35 \text{ dB} \tag{68}$$

If the tuning range is also considered, the tuning-range FoM can be calculated as:

$$\mathrm{FoM}_{\mathrm{T}} = \mathrm{FoM}_{\mathrm{jitter}} - 20\log_{10}\left(\frac{\mathrm{FTR}}{10}\right) \tag{69}$$

where FTR is the frequency tuning range in percent:

$$\mathrm{FTR} = \frac{f_{\max} - f_{\min}}{(f_{\max} + f_{\min})/2}\times 100\% \tag{70}$$

For the target PLL operating range from 2 GHz to 4 GHz, the frequency tuning range is:

$$\mathrm{FTR}_{\mathrm{PLL}} = \frac{4-2}{(4+2)/2}\times 100\% = 66.7\% \tag{71}$$

Thus, the tuning-range FoM based on the target PLL frequency range is:

$$\mathrm{FoM}_{\mathrm{T,PLL}} = -230.35 - 20\log_{10}\left(\frac{66.7}{10}\right) \tag{72}$$

$$= -246.83 \text{ dB} \tag{73}$$

If the full simulated VCO tuning range from 1.6 GHz to 4.2 GHz is used instead, the corresponding tuning range becomes:

$$\mathrm{FTR}_{\mathrm{VCO}} = \frac{4.2-1.6}{(4.2+1.6)/2}\times 100\% = 89.7\% \tag{74}$$

and the resulting tuning-range FoM is:

$$\mathrm{FoM}_{\mathrm{T,VCO}} = -249.40 \text{ dB} \tag{75}$$

These FoM results indicate that the proposed design benefits from the wide VCO tuning range. Even though the jitter is higher than some LC-VCO-based or aggressively optimized low-jitter PLLs, the design still provides a competitive trade-off when the wide 2 GHz to 4 GHz coverage, low power consumption, and compact ring-VCO-based implementation are considered together.

6. CONCLUSION

This thesis has presented a low-power dual-path sub-sampling PLL covering the 2 GHz to 4 GHz frequency range. The work was motivated by the need for a compact and power-efficient frequency synthesizer that can provide low-jitter clock generation while avoiding the large area and limited tuning range of LC-VCO-based solutions. A ring VCO was therefore adopted as the oscillator core, and its relatively high phase noise was addressed at the architecture level by using a wide-bandwidth sub-sampling PLL.

The theoretical analysis first compared conventional charge-pump PLLs with sub-sampling PLLs. In a traditional divider-based CPPLL, the phase detector, charge pump, and divider noise are strongly affected by the division ratio, leading to severe in-band noise degradation at multi-GHz output frequencies. By removing the divider from the main phase-locking path, the SSPLL avoids this fundamental noise multiplication for the SSPD and SSCP noise. The SSPD directly samples the high-frequency VCO waveform with the reference clock and provides a high phase detection gain around the zero-crossing point, which makes the charge-pump noise contribution much less critical. The noise analysis also shows that the VCO noise is shaped by a high-pass response and can therefore be suppressed more effectively when the loop bandwidth is increased.

Based on this principle, a dual-path SSPLL architecture was adopted. In addition to the conventional sub-sampling path, a high-pass-assisted path was introduced before the second SSCP. This path creates an additional zero-pole pair that extends the loop bandwidth while maintaining sufficient phase margin. As a result, the loop can suppress the ring VCO phase noise more strongly without sacrificing stability. To guarantee reliable acquisition, an auxiliary FLL with a dead zone and a TVC-based AFC scheme were also included. The AFC rapidly selects the proper VCO sub-band, while the FLL performs coarse frequency correction before the core sub-sampling loop completes the final phase locking. This staged locking procedure reduces the risk of false locking and enables fast acquisition over the full operating range.

The transistor-level implementation was designed in a 65-nm CMOS process. The main circuit blocks include a fully differential SSPD with isolation and dummy paths for reduced

charge sharing and loading variation, a duty-cycled SSCP with programmable pulse-width gain control, a current-starved three-stage differential ring VCO with coarse tuning and K_{VCO} trimming, a pulse-swallow divider, and the AFC building blocks including the T-Div3, O-Div3, TVC, and dynamic comparator. These circuit techniques were selected to balance noise, tuning range, locking speed, and power consumption.

Simulation results verify the feasibility of the proposed design. The VCO covers approximately 1.6 GHz to 4.2 GHz, providing sufficient margin for the target 2 GHz to 4 GHz range and for PVT variations. The simulated free-running VCO phase noise ranges from -110.6 dBc/Hz to -113.5 dBc/Hz at a 10-MHz offset. With the complete PLL operating at 2.05 GHz, the loop bandwidth is approximately 5 MHz, the phase noise reaches -111.357 dBc/Hz at a 10-MHz offset, and the integrated RMS jitter from 100 kHz to 100 MHz is 1.24 ps. The AFC completes its band-selection operation at about 387 ns, and the full loop settles in approximately 3 μs. The total power consumption is 6 mW at 2.05 GHz.

Overall, the proposed dual-path SSPLL demonstrates that a ring-VCO-based PLL can achieve a wide tuning range, low power consumption, and competitive jitter performance by combining sub-sampling phase detection, bandwidth-extension techniques, and fast digital-assisted frequency calibration. Future work may include post-layout extraction and verification, PVT and mismatch simulations, and further optimization of reference spur suppression and AFC robustness.

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