Model Based EMC:

A Qualitative assessment of Current Path Oscillations

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Lund University June, 2026

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Master's Thesis in Electrical Measurements

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Abstract

Electromagnetic compatibility (EMC) is essential for power electronic converters to prevent electromagnetic interference (EMI). Traditional post-design EMC testing is costly and time-consuming, motivating a shift toward model-based EMC (MB-EMC) with proactive EMI prediction. This thesis develops a simulation methodology for conducted emissions from an IGBT-based three-phase voltage source converter (3VSC) in the 150 kHz to tens of MHz range.

The converter's high-frequency behavior was examined under various grounding and component configurations using continuous operation and double-pulse tests (DPT). A sensitivity analysis identifies dominant parasitic coupling paths across frequency ranges. With a grounded heatsink, a common-mode path emerges, and heatsink parasitic capacitances and line filter inductors primarily determine lower-frequency oscillations in the 600 kHz range. Leaving the heatsink ungrounded shifts the lower-frequency oscillation to 1.35 MHz, which the model fails to reproduce, highlighting a differential-mode modeling gap.

At tens of MHz, oscillations are dominated by parasitic inductances, including unmodeled IGBT package inductances. Doubling modeled DC-link inductances as a proxy for IGBT package parasitics reduced the simulated resonance, improving measurement agreement. The DPT reduced average simulation time from 63.7 to 3.4 minutes, saving 60.4 minutes per test. This work provides a robust workflow for characterizing critical parasitics from board to package level, enabling early-stage conducted EMI prediction and a proactive power electronics design process.

Keywords: *Electromagnetic compatibility, conducted EMI, IGBT, parasitic capacitance, parasitic inductance, sensitivity analysis, double-pulse test, model-based design, common-mode, voltage source converter.*

Acknowledgements

We would like to acknowledge everyone who has assisted us in this work, offering their support, guidance and expertise throughout the project. We also want to express our gratitude to the hospitality and generosity we received at Comsys.

A special thank you to our supervisor at Comsys, Nils Lundström. Thank you for your patience and insights throughout the entire project. Your genuine interest and suggestions has helped us in many different areas of importance. Thank you Simon Lindvall and Oskar Siwerson for guiding us throughout different stages of our work.
A big thank you to our supervisor at IEA, Hannes Bydén. Your help and insightful suggestions were invaluable to us. Thank you for helping us with the measurements at LTH. A special thank you to our Examinator at BME, Johan Nilsson. Your help in seeing that our work meets the necessary standards were invaluable.

This thesis marks the completion of our studies in the Electrical Engineering program at LTH.

Contents

List of Abbreviations

CM	Common Mode
DUT	Device Under Test
DM	Differential Mode
DPT	Double Pulse Test
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
IGBT	Insulated Gate Bipolar Transistor
MB-EMC	Model-Based Electromagnetic Compatibility
PWM	Pulse Width Modulation
VSC	Voltage Source Converter
3VSC	Three-Phase Voltage Source Converter

1. INTRODUCTION

1.1. Background

Even in everyday electrical devices, from a car's infotainment screen to a factory robot, unwanted electrical noise can cause glitches or malfunctions which means that power electronics systems must operate reliably in their electromagnetic environments. Electromagnetic interference (EMI) is the disruption of an electronic device's operation caused by an electromagnetic field. Electromagnetic compatibility (EMC) is the ability of equipment to function correctly without generating or suffering the effects of this interference. Non-compliance with EMC standards such as CISPR 25, ISO (for automotive applications) and IEC (for industrial applications) can result in costly redesigns, certification delays or restrictions in major markets. Mitigating these risks necessitates a comprehensive understanding of EMI and EMC to ensure that electrical systems operate as intended (Rodriguez, 2012) (Sakthivel et al., 2003).

This thesis addresses conducted emissions from 150 kHz to several tens of MHz and focuses on insulated gate bipolar transistor (IGBT) based two level voltage source converter (VSC). This type of converter operates by rapidly and frequently changing the output voltage between two levels, which is known as switching. During switching, the converter's power semiconductor switching transitions generate high voltages and current slew rates (dv/dt and (di/dt). Sharp increases excite parasitic resonances in the main circuit and passive components which produce high frequency currents that propagate along the cables which can cause conducted EMI.

Average-value and fundamental frequency models suffice for power flow studies. However, these types of power electronics system models are not sufficient for capturing conducted emissions in the MHz range which demand detailed repre-

sentation of semiconductor switching transients, frequency-dependent parameters of passive components, and parasitic inductances and capacitances of the layout.

In order to address these challenges, this thesis combines simulation-based modeling with experimental validation using lab measurements which enables more reliable designs without over reliance on late stage prototyping. The goal of this thesis is to bridge the gap between theoretical modeling in simulations and real world EMI performance.

1.2. Thesis objectives

The objective of this thesis is to characterize electromagnetic behavior of an IGBT based converter in the 150 kHz - tens of MHz range by developing a validated simulation model and investigating the following reseach questions:

- How do different current coupling paths and stray components affect the dominant oscillation frequency?
- What are the main coupling paths for the system?
- How do stray component parameters influence the frequency content in the output current?

The goal in this thesis is to understand how the system, which is comprised of the converter under test and the simulation model, behaves under different testing configurations

1.3. Scientific contribution

This thesis contributes a validated modeling workflow for analyzing conducted EMI. By identifying dominant coupling paths and performing a sensitivity analysis on model parameters, this work provides a framework for bridging the gap between theoretical simulations and physical EMI measurements in power electronic converters.

1.4. Delimitations

This thesis focuses on measurements and simulation modeling of conducted EMI. Radiated emissions are beyond the scope of this thesis. The DC-link voltage is set to 48 V instead of 415 V (phase to phase) due to safety concerns.

1.5. Previous studies

This thesis would not be possible without prior studies done at Comsys on this topic. There are two master's thesis works that this thesis builds upon. The first is *EMC Modeling of IGBT-Based Voltage Source Converters: High-Frequency Behavior, Parasitic Characterization and Simulation Methodology* by Raväng, L and Siwerson, O (2025) which serve as our predecessors which means that this thesis directly builds upon their work. Their work presented a methodology for characterizing parasitic components in both passive and active circuit elements and provided a foundation for extending EMC modeling into higher frequency domains. The second thesis is *Model verification and common mode current analysis of grid connected three phase two level converters* by Lindvall, Simon and Haraldsson, Richard (2021). This work developed a high-frequency model of a shunt active filter that simulates common mode currents up to 2 MHz by using measured impedance and equivalent circuits to represent parasitic components, achieving its purpose and providing a foundation for further EMC analysis. These works serve as the foundation of this master's thesis and some of their results and experiences will be of use.

1.6. Project partners

This project was carried out primarily on-site at Comsys. Comsys is a company that specializes in developing active dynamic filters. The Department of Biomedical Engineering and Industrial Electrical Engineering and Automation have been involved in the thesis during the measurement of parasitic inductances.

1.7. Outline

The structure of the thesis is as follows:

Chapter 2 – This section covers the fundamental principles of EMC and EMI, alongside the high-frequency behavior of passive and active components. It further details the architecture and operation of VSCs, IGBTs and parasitic components.

Chapter 3 – Method: Outlines the equipment, procedures, and test configurations employed for both measurements and simulations. This encompasses the processes for impedance and junction capacitance measurements, along with the development of simulation models.

Chapter 4 - Results: Measurement and Simulation results as well as impedance data. Here simulation results are validated against measurements. Figures are first shown in order to show the reader what is analyzed and tables are used to present the results in an uncluttered manner such that readability is ensured.

Chapter 5 - Discussion: Results from the results section are discussed with the theory of EMC and EMI, alongside the high-frequency behavior of passive and active components. The methodology, measurement accuracy and simulation results are discussed. Furthermore, the thesis objective questions are answered and design guidlines for EMC in power electronic converters are discussed.

Chapter 6 - Conclusion: Main findings in the current oscillations paths and double pulse tests are summarized. Furthermore, future research has been discussed in order to further advance EMC methodology.

2. THEORY

This chapter establishes the theoretical foundation for the modeling of passive components and active semiconductors. Accurate representation of parasitic elements is essential for understanding electromagnetic compatibility (EMC) behavior in the 150 kHz to tens of MHz range. The following sections give a brief introduction to EMC and details the non-ideal characteristics of Insulated Gate Bipolar Transistors (IGBTs), culminating in the high-frequency equivalent circuit of the Device Under Test (DUT).

2.1. EMC and model based EMC

Model-based Electromagnetic Compatibility or *MB-EMC* is conceptually derived from the fundamental definition of electromagnetic compatibility, *EMC*. EMC is defined as the ability of an electrical or electronic device, system, or component to operate satisfactorily within its electromagnetic environment. The device must neither experience unacceptable interference from external electromagnetic disturbances nor generate emissions that could adversely affect the operation of other devices or systems. (International Electrotechnical Commission , IEC)

MB-EMC is a design approach in which simulations and models are used to study electromagnetic behavior instead of relying only on experimental testing. Engineers can predict and analyze how a device will behave in terms of electromagnetic emissions and immunity proactively during the design phase. This helps identify potential EMC problems early and reduces the need for costly redesigns later in the development process. (Baumgart, A ,Hormaier, K and Deuter, G , 2014).

It is important to note that MB-EMC is not limited to only internal effects within a device. While it can be used to study self-interference between components, it also allows engineers to evaluate how a device interacts with its surrounding

electromagnetic environment. This includes both the emissions that may affect other systems and the susceptibility of the device to external disturbances.

2.2. Electromagnetic interference EMI

Electromagnetic interference (EMI) refers to the phenomenon where the operation of one device or system is disturbed by electromagnetic emissions from another device, or in some cases, by emissions generated within the same device (self-interference). EMI can degrade performance, cause malfunctions, or even lead to complete system failure in sensitive electronic equipment.

Electromagnetic interference (EMI) may propagate through various paths and media to affect a susceptible system. Electrical connections, such as cables, as well as conductors in close proximity, can serve as coupling paths between systems. Interference transmitted through direct electrical connections is classified as conducted EMI, whereas inductive and capacitive EMI result from coupling via time-varying magnetic and electric fields, respectively.

Electromagnetic interference (EMI) can be classified into four main types. Conducted interference propagates through electrical connections, such as cables and power lines. Radiated interference is transmitted through electromagnetic fields in free space. Inductive interference arises when two conductors are separated by a distance smaller than a wavelength, enabling coupling through a time-varying magnetic field. In contrast, capacitive interference occurs due to the presence of an electric field between two conductors that are likewise spaced at less than a wavelength. Typical sources of EMI include switching power supplies, wireless communication systems, and high-speed digital circuits (Taranovich, 2023).
EMI is considered the problem that electromagnetic compatibility (EMC) aims to control. While EMI represents unwanted electromagnetic disturbances, EMC focuses on ensuring that devices can operate correctly in their electromagnetic environment without causing or being affected by such interference.

2.3. Conducted current modes

Two important aspects of EMI are studied in this project: differential mode and common mode.

Differential mode *(DM)* occurs when noise currents travel in opposite directions along a pair of conductors or, in the case of this study, three conductors; this is referred to as DM EMI. In this case, the noise current flows out on one conductor and returns on the paired conductor, forming a closed current loop rather than flowing through ground. DM EMI depends heavily on the loop area: small loops radiate less, while larger loops radiate more due to the stronger magnetic field generated by the current loop. Therefore, in EMC design, the loop area should be minimized to reduce differential mode noise and radiated emissions. DM EMI is primarily classified as conducted interference, although electric-field coupling between conductors can also contribute to the overall EMI behaviour (Williams, 2016, p.270-271),(Paul et al., 2022, p.398)

Common mode *(CM)* refers to noise currents flowing in the same direction through one or more conductors and return through an unintended path such as ground. This type of noise is typically caused by parasitic capacitance in combination with high frequencies. It forms large current loops and can turn cables into antennas that radiate EMI. One of the most effective methods to reduce CM noise is the use of a common-mode choke, which employs magnetic cores to suppress these unwanted currents. CM EMI can be classified as a type of conducted EMI, as it propagates along wires and cables. It is frequently associated with capacitive as well as inductive coupling, where high-voltage transients couple through parasitic capacitances to ground. Because CM EMI is categorized as capacitive EMI, it can occur even in non-switching environments. The capacitive coupling path are present even without switching; however, the

problem becomes more severe in switching applications and at higher frequencies. (Williams, 2016, p.271),(Paul et al., 2022, p.398-399).

2.4. EMC Modeling of various electronic components

Electronic components such as capacitors, inductors, IGBTs, and even resistors have behaviors that are highly dependent on frequency. At low frequencies, from a few hertz up to several kilohertz, these components generally operate as intended, and EMC considerations are minimal. However, at higher frequencies from around 20 kHz up to several megahertz almost all electronic components exhibit different behavior due to parasitic effects. In this frequency range, component modeling must account for these parasitics to properly assess EMC. In this section, an introduction to the components and their corresponding EMC-oriented modeling is presented.

2.4.1. IGBT

An IGBT (Insulated Gate Bipolar Transistor) is a high-efficiency power semiconductor device that can be easily switched by applying a voltage to the gate while handling high current and voltage levels. It is widely used in applications such as inverters, electric vehicles, and power supplies.

Figure 1 shows the high-frequency model of an IGBT, where the capacitance between the collector and gate is denoted as C_{GC}, between the gate and emitter as C_{GE}, and between the collector and emitter as C_{CE}. In a laboratory environment, it is not possible to measure these capacitances individually; that is, C_{GC}, C_{CE} and C_{GE} cannot be measured separately. Instead, the capacitances that can be measured in practice are C_{res}, C_{oss} and C_{ies} which are defined in equations (1), (2) and (3).

$$C_{ies} = C_{GE} + C_{GC} \tag{1}$$

$$C_{oss} = C_{CE} + C_{GC} \tag{2}$$

$$C_{res} = C_{GC} \tag{3}$$

C_{ies} is also called input capacitance, measured between the gate and the collector–emitter terminals after the collector is shorted to the emitter. C_{oss} is the output capacitance, measured between the collector and gate terminals after shorting the gate to the emitter. Finally, C_{res} is the reverse transfer capacitance, measured between the collector and gate while the emitter is grounded. (Raväng, L and Siwerson, O, 2025)

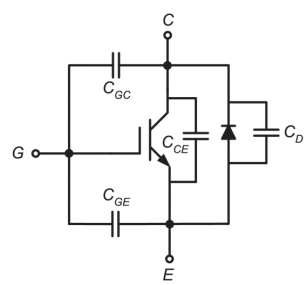


Figure 1: IGBT circuit model with parasitic capacitances included (Hizarci ,H. Pekperlak ,U. Arifoglu ,U., 2023)

2.5. ADF 25 and main components of the Device Under Test DUT

The ADF P25 is an active dynamic filter with a switching frequency of $f_{sw} = 20$ kHz. Active This filter serves as the reference unit for all measurements made and is the Device Under Test (DUT). The specific ADF P25 used has the notable feature of having separate heat sinks for each of the three half-bridge power modules (Comsys AB, 2025), however the heatsinks have been joined together for the measurements and simulations.

The ADF P25 is an active dynamic filter designed to eliminate all current components that do not contribute to active power, such as reactive power and harmonic distortion. As illustrated in Figure 2, when a load is connected to the grid, it draws a load current represented by the red waveform. The ADF P25 injects a compensating current, shown by the dark blue waveform, which counteracts the reactive and harmonic components introduced by the load. As a result, the grid current becomes a smooth sinusoidal waveform, represented by the light blue curve.

The operating principle of the ADF P25 is analogous to that of noise-cancelling headphones. In a similar manner, the filter generates a compensating waveform that is equal in magnitude but opposite in phase to the unwanted components, thereby cancelling them and leaving only the desired signal.

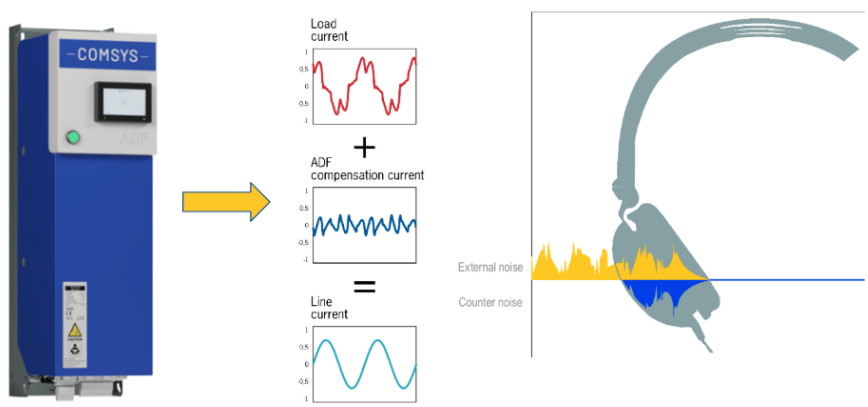


Figure 2: Illustration of the ADF P25 and its functionality.

In this section, the circuit diagram of the AC/DC converter—also referred to as the DUT used in this thesis is introduced. Figure 3 shows the low-frequency model of the converter, where no parasitic capacitances are included in the diagram. In Figure 3, the circuit is divided into four main parts: the battery and DC link, the three phase converter, the LCL filter, and finally the load.

Battery and DC link The battery and DC link form the input DC side of the converter and consist of two batteries, each rated at 24 V. The DC link consists of capacitors that are essential for smoothing out fluctuations in the DC voltage and for providing a low-impedance path to the IGBTs in the next stage.

Three phase converter In this stage, the conversion from DC to AC takes place. As shown in Figure 3, the converter consists of six IGBTs, where each leg is made up of two IGBTs, one upper and one lower, that together generate one phase of the AC output from the DC input. Additionally, each IGBT is equipped with an antiparallel diode. These diodes are essential for providing a path for the current when the IGBTs are switched off, allowing for freewheeling of inductive currents and ensuring proper operation of the converter.

L-filter The L filter is located on the output side of the converter, where it smooths the AC signal before it reaches the grid. The signal prior to the L-filter contains high-frequency ripples caused by the switching of the IGBTs. These ripples are attenuated by the L-filter, resulting in a smoother sinusoidal waveform suitable for injection into the grid.

The load Finally, the load consists of resistive elements that emulate a load in practice. In a real system the grid is not purely resistive but consists of complex impedance including both inductive and resistive components.

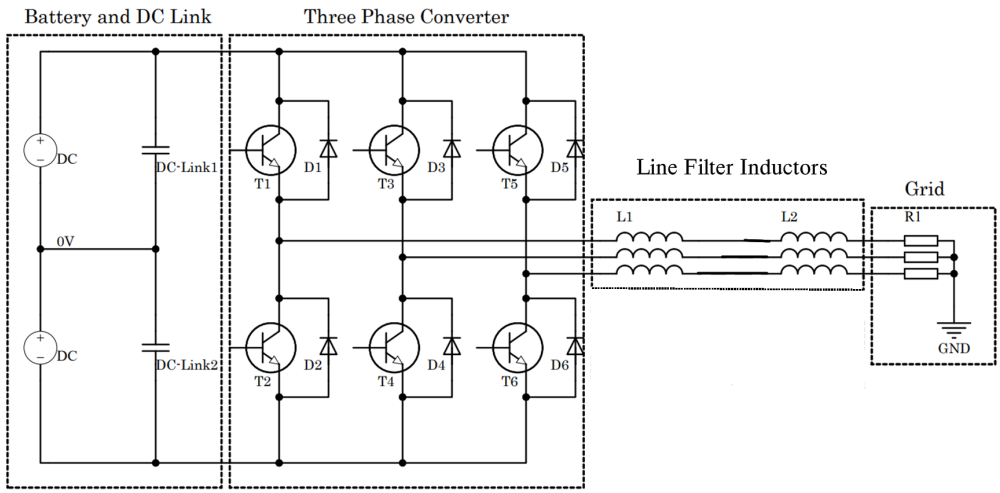


Figure 3: Circuit diagram of the DC/AC conveter known as conveter under test

2.6. Normal operation and double pulse test

In this thesis, two types of operations have been investigated, Normal operation and double-pulse test:

Normal operation: The Normal operation investigated in this thesis can be simply described as the normal operation of the converter over a limited period of time. The switches are controlled to operate for a specified duration, determined by the operator through a control system managed by software. The result is an AC signal generated from a DC input.

During operation, the switches are turned on and off rapidly using a control method called pulse width modulation (PWM). Each phase has its own leg, and each leg consists of two IGBTs. These two IGBTs must never be turned on at the same time, as this would cause a short circuit across the DC link, instead, the IGBTs in each leg are switched on alternately, ensuring safe and proper operation of the converter.

One period of the AC output signal is divided into multiple switching intervals. Switching periods are illustrated in figure 4. In the first switching interval,

switches T1, T4, and T5 are turned on. This causes current to flow out through phases 1 and 3 and return through phase 2 which results in the sum of the DM currents in phases 1 and 3 is equal to the current in phase 2. In the second switching interval, switches T1, T4, and T6 are turned on simultaneously. In this case, current flows out through phase 1 and returns through phases 2 and 3. Therefore, the sum of the currents in phases 2 and 3 equals the current in phase 1. This switching sequence continues through different combinations of switches, forming a complete cycle that approximates a sinusoidal AC output.

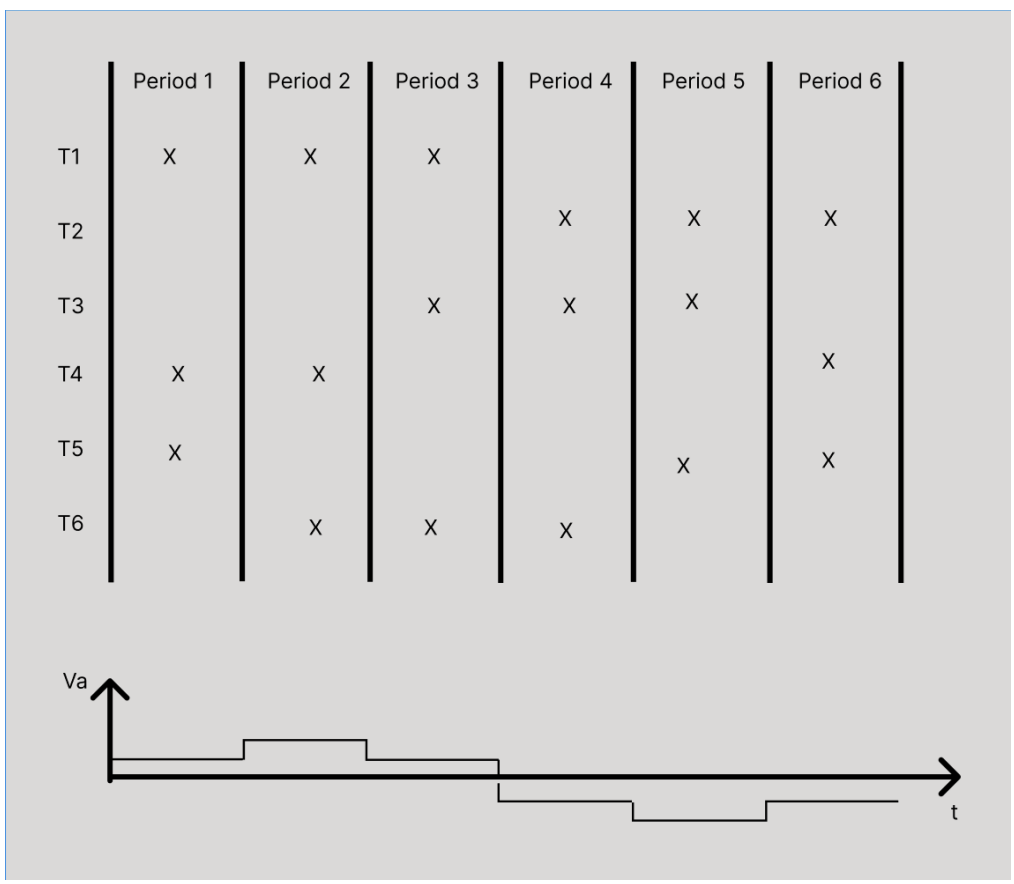


Figure 4: Illustrative figure showing 6 switching periods

Double pulse test: The double pulse test is another test performed on the DUT. Unlike Normal operation, the purpose of the double pulse test is not to demonstrate the behavior of the entire converter, but rather to analyze the

switching characteristics of the devices themselves. This operation is controlled by a separate control system and software, where the operator can define which switches are activated and for how long.

In this operation, the switching process goes through three intervals. The first interval, known as the current build-up interval and marked as number 1 in figure 5, occurs when the intended switch is on. Current flows from the DC+ terminal through the switch, charges the inductor, and returns to the DC- terminal. The second interval begins when the switch is turned off after the first pulse. This interval is marked as number 2 in figure 5. The current stored in the charged inductor continues to flow through the diode of the opposite switch in the same leg before returning to the DC+ terminal. The final interval occurs when the switch is turned on again, marked as number 3 in figure 5. During this interval, the switching characteristics of the device, such as the turn-on behavior and the switching losses, are observed.

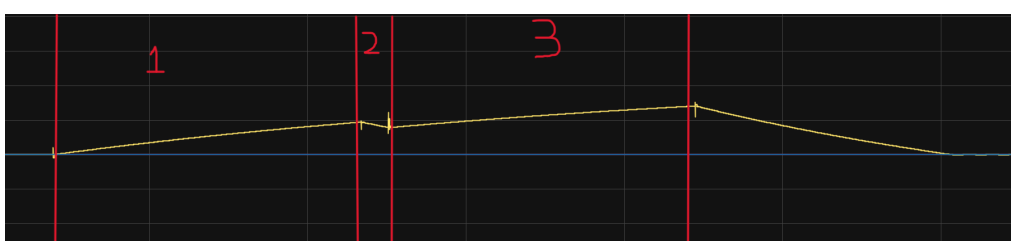


Figure 5: Illustrative figure showing DPT current

3. METHOD

This chapter presents the methodological framework employed to investigate the conducted EMI characteristics of the IGBT-based VSC. The approach combines experimental measurements with simulation-based modeling to enable validation and analysis of parasitic phenomena. A systematic four-phase workflow is described, followed by detailed descriptions of the test rig, measurement procedures, simulation model development, and specific testing methodologies including double pulse testing and parasitic inductance characterization.

3.1. Method overview

The methodology follows a systematic four-phase approach designed to progressively identify, validate, and analyze parasitic elements affecting model accuracy.

Phase 1: Baseline Characterization — Measurements of the DUT were performed under two different grounding configurations: the heatsink of the DUT was alternately grounded and ungrounded which can be seen in Figure 7 under the ADF P25 caption. These measurements established an experimental baseline against which simulation results could be compared.

Phase 2: Model Development and Initial Comparisons — Simulation model development incorporated measured parasitic parameters from prior work conducted on the same DUT. Initial simulations were compared with baseline measurements to identify discrepancies and guide further model refinement.

Phase 3: Sensitivity Analysis and Parameter Identification — Systematic variation of model parameters was performed to identify which parasitic elements exert the greatest influence on oscillation frequency and current path behavior. This phase enabled the identification of dominant capacitive coupling paths.

Phase 4: Validation and Configuration Testing — The refined simulation model was validated against measurements across multiple test configurations,

including variations in inductance, added capacitances, and snubber configurations.

3.2. Modeling of the DUT in the 150 kHz - tens of MHz range

The parasitic capacitances shown in the circuit diagram in figure 6 are the ones investigated in this project.

Model of battery and DC link

The cable that connects the batteries to the DC link is modeled as inductance as shown in Figure 6. The DC link inductances are modeled by adding inductances for each phase labled as L-DClink, located at the connection between the DC link and the IGBTs.

Three phase converter

In the three-phase converter section of the circuit diagram, the IGBTs are modeled to include the parasitic capacitances which become more significant at higher frequencies. C_DC+, C_DC- and C_AC represent parasitic capacitances between the heatsink and the power module. In this diagram, DC+, DC- and AC are grounded, which corresponds to grounding the heatsink. In this project, two different configurations are investigated: one in which the heatsink is grounded and one in which it is not. This will be examined further in the report.

The filter and load were modeled as ideal elements as these were not investigated in this report.

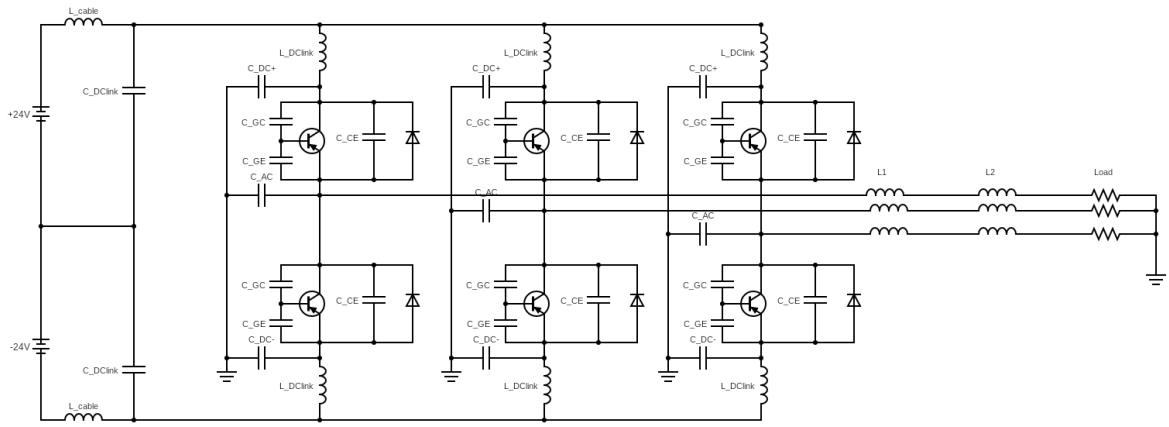


Figure 6: Circuit diagram of the DC/AC converter of the DUT with parasitic capacitance present

3.2.1. System configuration

The complete test setup consists of the following components:

- ADF P25 which is the DUT
- DC Power supply configured for 48 V operations
- Line filter inductors(s)
- three phase 50 Ω resistors
- The controller circuit which connects to a computer
- Oscilloscope
- Oscilloscope probes for measuring voltages and currents

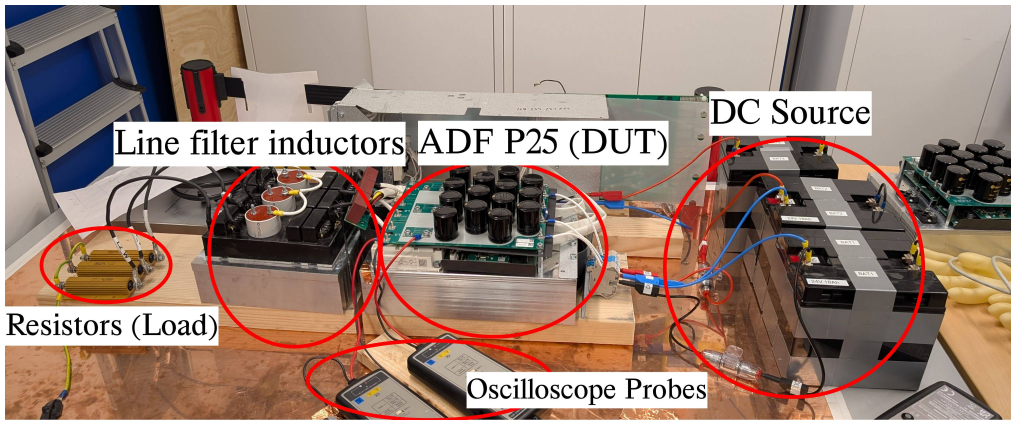


Figure 7: Lab setup with the DC source, complete DUT and the 50 Ω resistors. This is the ungrounded configuration where the DUT is ungrounded

3.2.2. Measurement equipment

The oscilloscope used is a Rohde & Schwarz RTB2004 which is a 4 channel oscilloscope with a bandwidth of 70-300 MHz, a maximum sample rate of 2.5 GSa/s and a 10 bit A/D converter. The oscilloscope probes used for measuring voltages are active differential oscilloscope probes called Pico Technology TA042 with a 100 MHz bandwidth. They can measure voltages up to ±1400 V (DC + peak AC). The current probe used is a current wave transducer called CWTMini50HF/06 from PEM.

3.2.3. Testing configurations

The test rig supports multiple different configurations to adress the research objectives. These configurations are divided such that grounding configuration of the DUT heatsink is the main category. And configurations like inductance variations, IGBT capacitances, snubber capacitances and controller are considered subcategories. This is because the two DUT grounding configurations have different current paths. The purpose of these categories is to make it easier to navigate the report.

For the purposes of this investigation, two different grounding configurations were implemented. Those being:

- **Grounded Heatsink Configuration**: where the heatsinks of the DUT directly connected to ground.
- **Ungrounded Heatisnk Configuration**: were the heatsinks of the DUT are isolated from ground.

These configurations allow for systemic investigation of how parasitic elements (capacitances and inductaneces) affect oscillation behaviour and overall EMC performance.

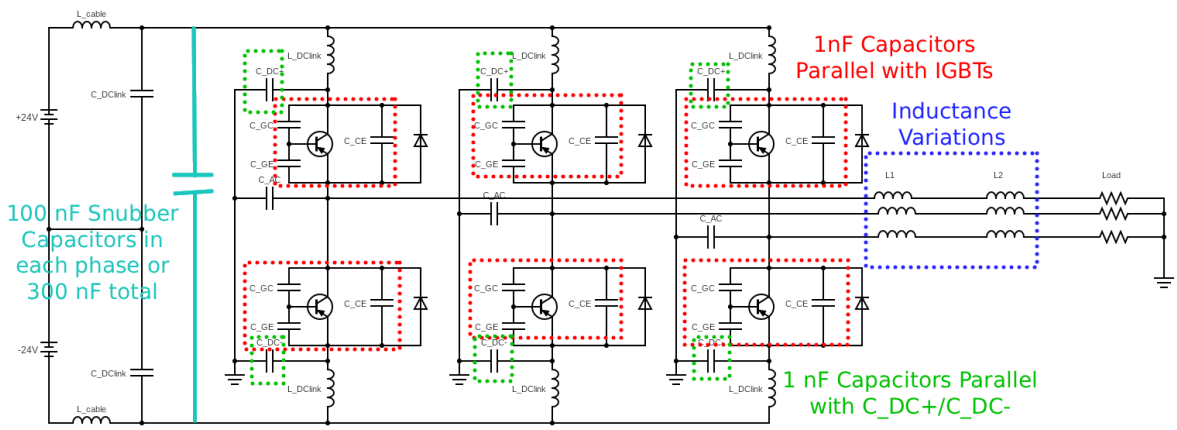


Figure 8: Circuit diagram (with grounded DUT heatsink) featuring which circuit elements are affected from the configurations

Table 1: Overview of investigated configurations

Configuration category	**Specific configuration(s)**
Inductance variations	**Standard configuration (baseline)** – Figure 7 **Additional filter inductance is connected in parallel** with L1 and L2, reducing the effective output inductance with a factor 2 **Additional filter inductance is connected in series** with L1 and L2, increasing the effective output inductance with a factor 2
Capacitor in parallel with IGBT configurations	Added 1 nF capacitors in parallel to the IGBT collector and emitter terminals in each phase. This is done either on the IGBTs on the DC+ side or on the DC- side.
Capacitors in parallel with parasitic heatsink capacitances	Adding 1 nF snubber capacitors parallel with C_DC+ or C_DC- in each phase
Adding 100 nF snubber capacitors between the DC+ and DC- terminals for each phase 3VSC	

In order for the reader to understand how much the reactive components are affected by the configurations in Table 1, the component values are presented in Table 2

Component	Value
L1	61.4×10^{-6} H
L2	16.66×10^{-6} H
C_DC+	347×10^{-12} F
C_DC-	78×10^{-12} F
C_AC	411×10^{-12} F
L_DClink1	10×10^{-9} H
L_DClink2	8.2×10^{-9} H
L_DClink3	9×10^{-9} H
C_{GE}	16.4×10^{-9} F
C_{CE}	0.02×10^{-9} F
C_{GC}	1.15×10^{-9} F

Table 2: Component values for the circuit.

3.2.4. Measurement considerations

Careful thought was taken to ensure that the oscilloscope probes had proper placement and grounding, bandwidth settings of the oscilloscope and minimizing interference from the measurement equipment.

3.3. Measurement procedure

The measurement procedure was designed in such a way that oscillation behaviour could be captured under various test configurations. This way repeatibility and low measurment errors could be ensured so that the procedure follows a structured approach divided into several different phases.

3.3.1. Pre-measurement setup

Before any measurements were made, the following preparation steps were made. Firstly, the measurement equipment, those being the oscilloscope, oscilloscope probes and controller circuit connected to a computer, were verfied by checking for proper operation.

- Both the oscilloscope and oscilloscope probes' damping were set to 1:100 so that the measurements are accurate for voltages and currents are accurate.
- Oscilloscope bandwidth settings were configured appropriately for the expected frequency ranges of 600 kHz-1.8 MHz and tens of MHz. The sampling frequency for the oscilloscope was 1.25 GSa/s for all measurements
- Each time a new measurement was being made, the amount of samples being captured and current are at first made to be low by using the controller circuit. Then, gradually, the current was made higher and the signal period was made longer. This was done in order to ensure a signal was seen on the oscilloscope without straining the equipment as well as ensuring safety.

3.3.2. Measurement points

Voltage measurements were taken at two different points. The first one was taken at the output of the three phase voltage source converter, specifically the voltage between the output of one of the phases and ground. The second voltage measurement was taken over one of the IGBTs' collector and emitter terminals. The IGBT in question is on the same phase as the voltage as the output voltage. A current measurement was also made through the output of the same output terminal the 3VSC.

3.3.3. Measurement procedure steps

After the pre-measurement steps were fulfilled, measurements were made on the measurement points (see 3.3.2). This is done by first supplying the 48 V DC source to the circuit as seen in for example figure 7. Then the controller circuit is turned on by supplying 24 V DC.

Using the computer connected to the control circuit, measurements could be made by controlling the input current and sample count. Currents of 0, 5 A and 10 A were being used as well as a sample count of 100-10000. The measurements saved in the results were made using 5-10 A and 1000-10000 samples. The reason for this variance depends on the measurements being made.

3.4. Simulation setup and models

The simulation model used and developed is based on Matlab/Simulink. During this thesis work Matlab (2024b) and Simulink were utilized along with the toolboxes Simscape, Simscape Electrical, DSP system toolbox and Signal processing toolbox version 24.2.

3.4.1. Simulation model

The simulation model was developed based on the model from Raväng, L and Siwerson, O (2025) and the circuit found in Figure 6. If the reader wants to see the simulink models in the Matlab environment, you are referred to figures 35 and 36 in 6.1. The purpose of the development of this new model developed by us is to simplify the model, to obtain a controlled environment, introduce more accurate parasitic elements and to shorten simulation times.

The model was developed to include parasitic inductances that come from the DC-link capacitors on the IGBTs. This was done to make the model more accurate, Parasitic inductances have been put into each leg of the three phase voltage source converter circuit. Using the simulation model, simulations were carried out with the different configurations found in 3.2.3 and variation in DC-link parasitic inductance. By varying different parameters, a sensitivity analysis is made. This was done for the sake of analyzing current path oscillations and the dominant and non-dominant capacitances. The results were then compared to the measurements which were done using the measurement procedures found in 3.3.

3.5. Double pulse test

In this thesis, the DPT is used to address a major issue, namely the time-consuming simulations associated with continuous operation. Two pulses are analyzed, which can potentially give higher resolution on the simulation since the testing is only done at a fraction of the time of the previous two simulations and only one phase is tested. This means less calculations done in the simulation. Since this work focuses on model-based EMC, the most important aspect of the signal to analyze is the resonance frequency caused by the parasitic capacitances described earlier. This phenomenon is present in both continuous operation and

double pulse testing. Therefore, the double pulse test allows for a simplified model and significantly faster simulations, while still providing equivalent results.

3.5.1. Double pulse testing measurements

The measurement procedure of the double pulse test does not differ entirely from that used in the continuous operation case. The only difference between them is the control circuit and software. The software is primarily designed to allow the operator to control specific switches for defined time intervals during each switching period, as described in the theory used for this operation.

The model used in the double pulse operation is the same as that used in the continuous operation; however, the difference lies in how the model is controlled. In this case, the controller is used to operate specific switches for defined periods of time. Figure 11 illustrates which IGBTs are switched on and which remain off during operation.

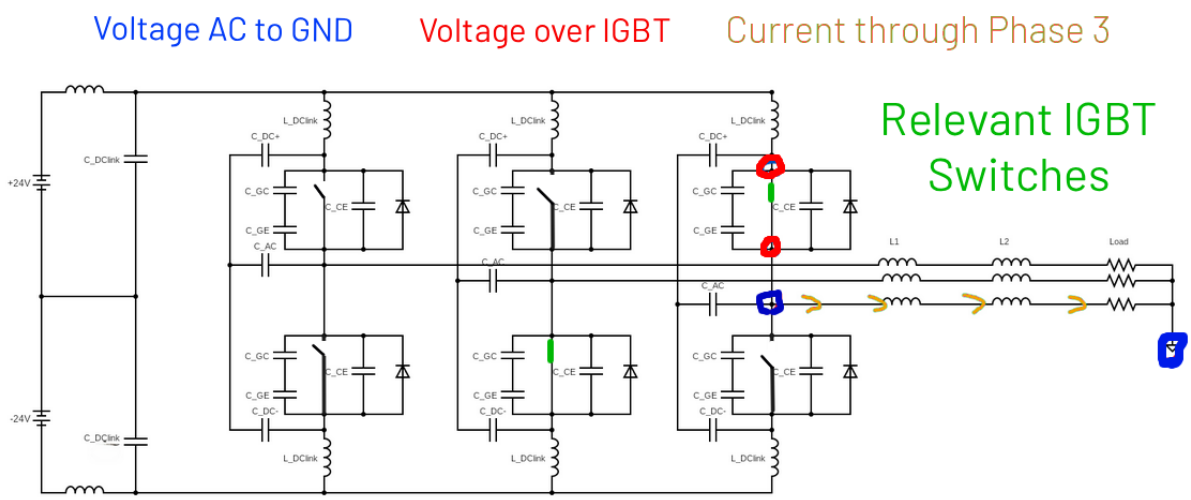


Figure 9: Model of DPT during operation with measurement points. During operation, the switches marked green are the ones operating, while the ones marked black are not switching

As shown in Figure 9, two IGBTs were selected for switching: the bottom IGBT in phase 2 and the top IGBT in phase 3.

The measurement points shown in Figure 9 include the AC output of the third phase, as well as the voltage across the top and bottom IGBTs in the same phase. The voltages across the IGBTs were measured to ensure proper switching operation and to analyze the resonance frequency, similar to the approach used in the continuous operation case.

3.5.2. Double pulse testing simulations

The same simulation model has been used with some modifications.

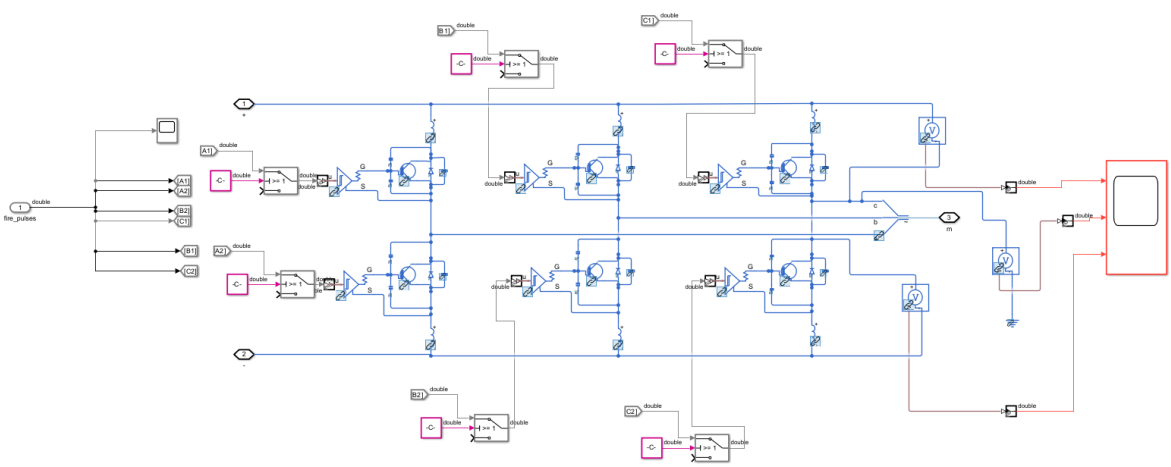


Figure 10: Part of the DPT simulation model, IGBT block

Each IGBT shown in Figure 10 is controlled separately using a MATLAB script, allowing a pulse to be applied and the device to be switched on for a defined period of time, similar to the procedure used during the measurement process. The same signals are measured to obtain results comparable to those from the physical measurements.

The double pulse test simulation and the simulation using three phase operation are compared in regards to simulation times in order to show how much potential time can be saved. By taking five different simulations for the same scenarios (Default case with Grounded heatsink) and calculating the average time it takes for the simulations, simulation times can be compared. The results shown in table 9 in section 4.3.

3.6. Limitations of the model

A central assumption in this thesis is that the most critical aspect of the signal for electromagnetic interference is the resonance frequency caused by parasitic capacitances and inductances in the circuit. While this approach is valid for analyzing the specific ringing phenomena observed, it is important to acknowledge a key limitation: the model does not account for the broadband frequency spectrum inherent to the signal's own waveform, which is an independent and significant source of interference.

Even a theoretically perfect square wave, completely free of the oscillations that would be damped by a zero-inductance circuit, possesses a frequency spectrum defined by its Fourier series. The amplitude of the harmonic components in this spectrum is fundamentally governed by the signal's rise and fall times (t_r, t_f) which can be seen in figure 11.

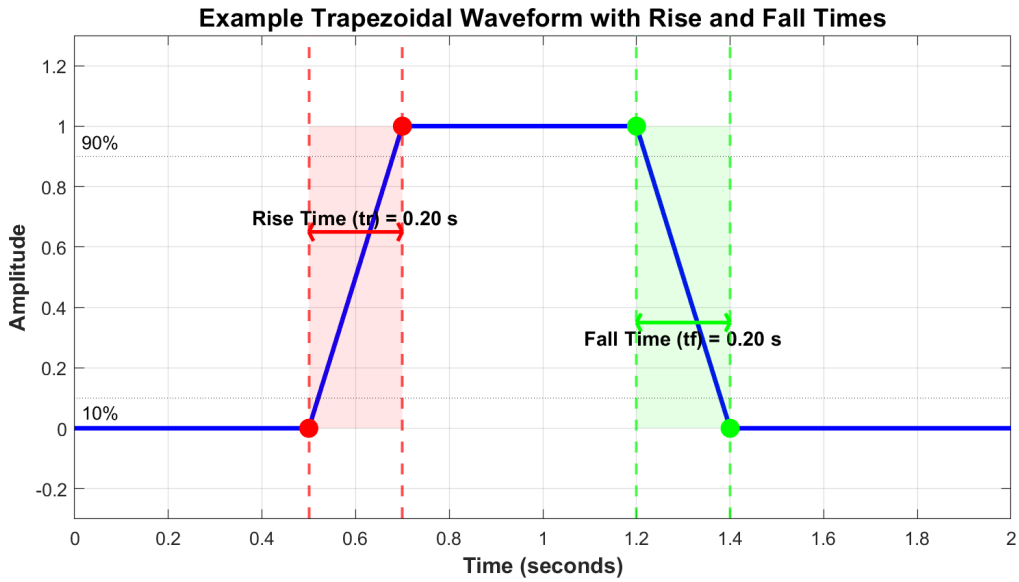


Figure 11: Trapezoidal square wave with the rise and fall times highlighted

Faster switching transitions correspond to a higher amplitude of high-frequency harmonics. These harmonics can propagate through radiated, capacitive, or inductive coupling paths, causing electromagnetic interference in neighboring circuits, irrespective of any resonant behaviour within the source circuit itself.

This coupling mechanism is not captured by the current model, which focuses solely on discrete resonance frequencies arising from parasitic LC tanks. As a result, the analysis may underestimate the total interference potential in systems where the driver's rise/fall time is very short. The interference generated by the first few tens of harmonics of the fundamental switching frequency, for example, could be significant but is not predicted by the resonance analysis performed here. Future work should integrate a time-domain analysis of the switching waveform's slew rate to provide a more complete picture of the system's electromagnetic compatibility, combining both the resonant and broadband spectral contributions to interference.

3.7. Parasitic Inductance from the DC-link capacitors

To parametrize the model of the DC-link capacitors, measurements were made using an impedance analyzer. The Hioki IM7581 is used measurements between 100 kHz and 15 MHz. The measurement of importance in this case is parasitic inductances on the terminals of DC+ and DC-. These inductances originate from the DC-link capacitors that sit on top of the IGBTs including the DC-link capacitor circuit board.

3.7.1. DC-link capacitor circuit model

Figure 12 shows the DC-link capacitor circuit. The terminals of interest are DC+ and DC- terminals. These are of interest since there is one IGBT for each DC link terminal.

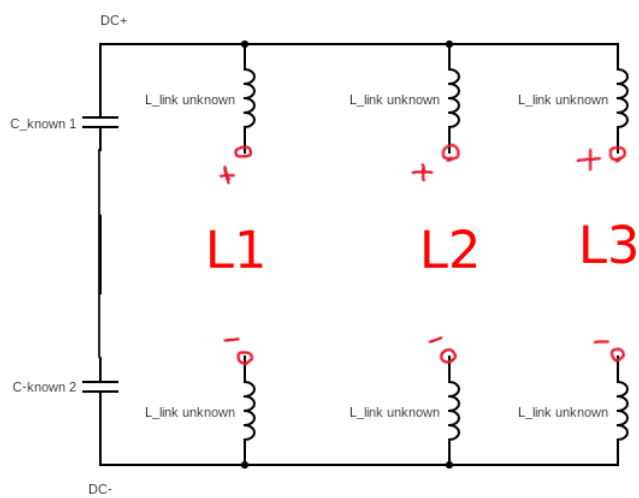


Figure 12: Circuit for caclulating Link inductances. IGBTs are removed since the terminals being measured are where the IGBTs used to be. The highlighted terminals are the measurement points. Note that there are three inductance measurements, one for each phase which corresponds to each leg of the 3VSC

From the circuit in figure 12 it is seen that every measurement is a measurement of two parasitic inductances on each leg of the 3VSC. This means that three

measurements are needed and each inductance measurement is an addition of two unknown parasitic inductances.

Figure 13 shows a photograph of the DC-link capacitor bank.

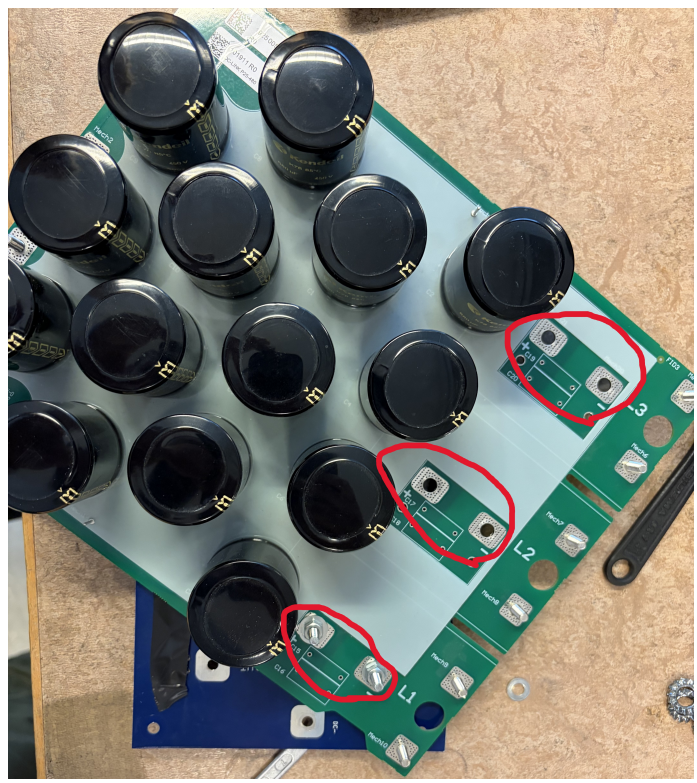


Figure 13: DC-link capacitor circuit board which corresponds to the circuit found in figure 12 for caclulating Link inductances. The highlighted terminals are the measurement points

3.7.2. Inductance measurements

Inductance was measured using an impedance analyzer. The impedance analyzer calculates the inductance in a stepwise manner. Step 1 is: The phase angle can be used to determine the reactance X from the measured impedance magnitude $|Z|$ and phase angle θ, since $X = |Z| \sin \theta$.

However, to go from reactance to inductance, two assumptions must be made. The first assumption is that the reactance is purely inductive, meaning the capacitive contribution is neglected entirely. This is equivalent to dropping the $-\frac{1}{\omega C}$ term from the complex impedance equation:

$$Z = R + j\left(\omega L - \frac{1}{\omega C}\right). \tag{4}$$

Under this assumption, the impedance simplifies to:

$$Z = R + j\omega L. \tag{5}$$

The second assumption concerns the equivalent circuit topology. Equation (5) implicitly assumes a series connection of R and L, yielding $Z = R + j\omega L$. If the resistance and inductance were instead connected in parallel, the impedance would be

$$Z = \frac{R \cdot j\omega L}{R + j\omega L}, \tag{6}$$

which has a different frequency dependence. One must therefore examine how the measured impedance varies with frequency to justify whether a series or parallel model is appropriate for the three inductances referred to as L_1, L_2, and L_3. Measurements are made between the frequencies 100 kHz and 15 MHz with 801 samples between these frequencies.

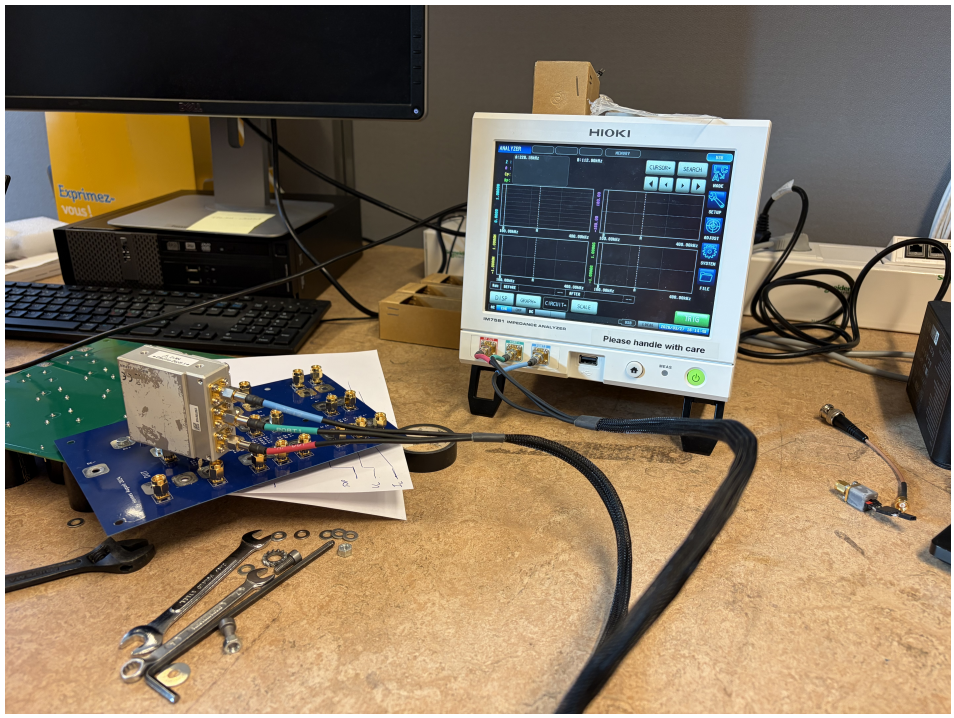


Figure 14: Measurement setup for Link inductances. Pictured are the impedance analyzer, DC-link circuit and measurement circuit

Since the parasitic inductances from the DC-link circuit are modeled such that there are six different inductances (one for each leg) as in figure 12, the simulation model will use the values of each phase inductance divided by two for simplicity. Furthermore, the inductance value will be an average of of the inductance values for the sake of maintaining short simulation times and maintaining simplicity since using a linear inductance value that changes depending on frequency leads to higher simulation times. Choosing link inductance this way is viable, as there is not much variance in inductance between frequencies. Keep in mind that the impedance analyzer works best on 50 Ω while measurements in this case were done on a few mΩ which might skew the measurement results.

4. RESULTS

4.1. Link inductance and impedance measurements

The results of the DC-link inductance measurements are presented. The following measurements are made with a HIOKI IM7581 impedance analyzer.

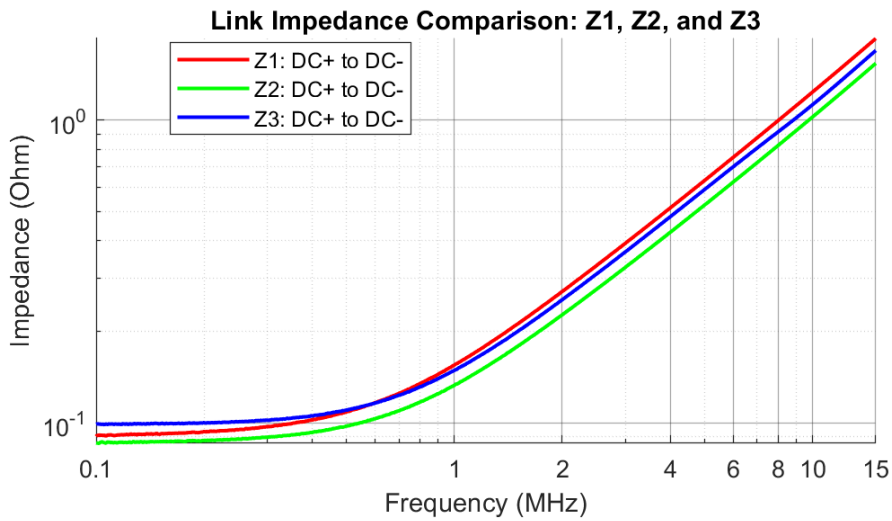


Figure 15: DC-link Impedance measurement plots for all three phases for the frequencies 150 kHz to 15 MHz

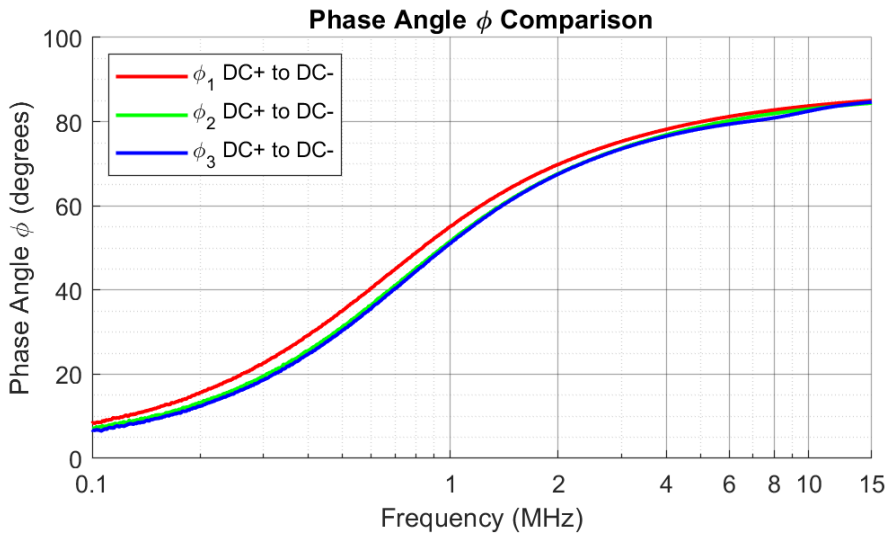


Figure 16: Phase angle measurement plots for all three phases for the frequencies 150 kHz to 15 MHz

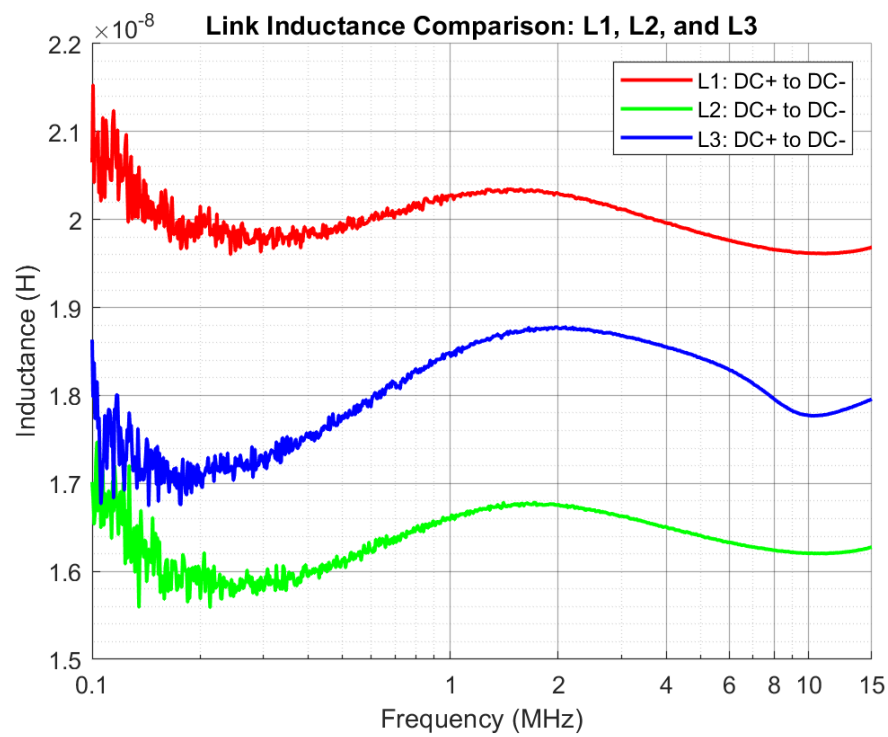


Figure 17: Link Inductance measurement plots for all three phases for the frequencies 150 kHz to 15 MHz

Table 3: Link Inductance maximum, minimum and average values for each phase

Link Inductances	L1 (nH)	L2 (nH)	L3 (nH)
Max	21.6	16.7	18.8
Minimum	19.6	15.6	16.8
Average	20	16.4	18

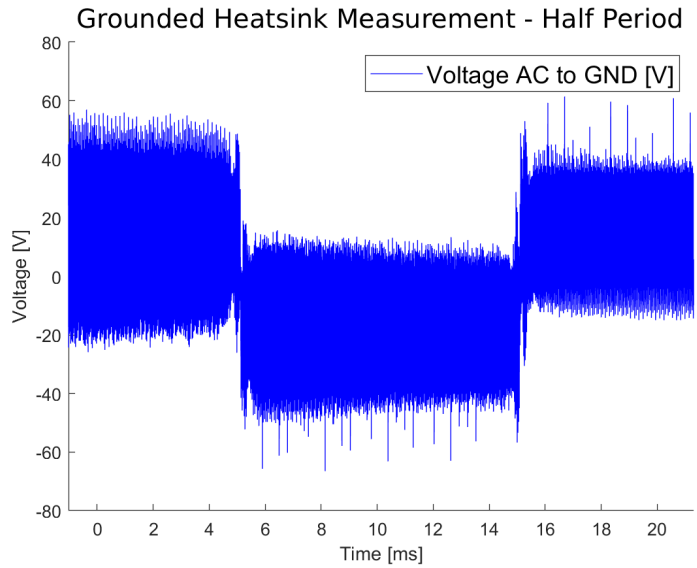
Keep in mind that the values in table 3 are the sum of the entire phase, which means that these inductance values must be divided in two for the six link inductances.

4.2. Current path oscillations, dominant capacitances and sensitivity analysis

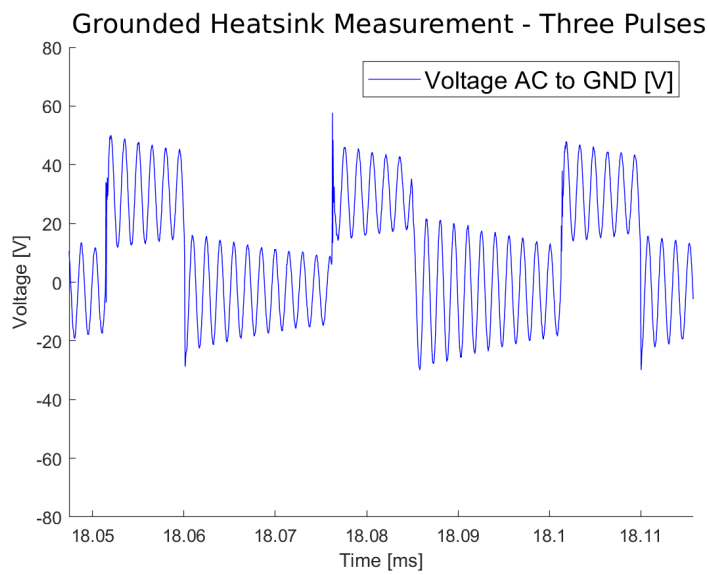
In order to analyze current path oscillations and dominant and non-dominant capacitances, measurements and simulations were made using multiple different testing configurations with the measurement procedures outlined in 3.3. These configurations are those discussed in 3.2.3. The configurations are divided such that the grounding configurations of the DUT heatsink are the main categories. What are considered subcategories are line filter inductance configurations, snubber capacitor configurations, added capacitors in parallel with IGBTs. To understand which parts of the circuit that are affected, refer to Figure 8 and Table 1. Both measurements and simulation results for each configuration are shown in the same parts in order to make comparisons between simulations and measurements easy.

Since the figures are so similar across different configurations, one simulation figure and one measurement figure will be provided in order for the reader to get an idea of how the simulation looks like and which values are of importance to keep the report streamlined and uncluttered.

4.2.1. Lower frequency range oscillations (600 kHz - 1.8 MHz)

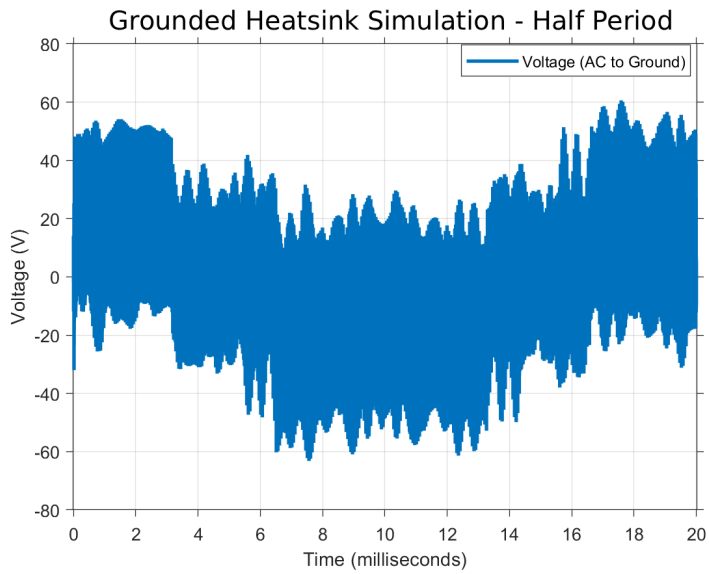


(a) Overview of voltage (AC to GND) measurement result (half period)

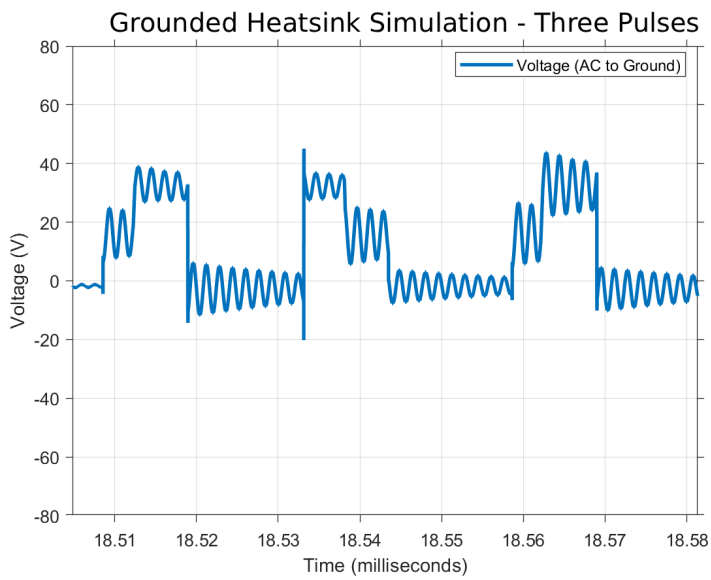


(b) Zoomed in (x-axis) to show three pulses of the measurement results

Figure 18: Measurement results from three phase operation featuring the Voltage from AC to ground using the Default Case, grounded heatsink. The frequency of visible oscillations in figure 18b is 667 kHz.



(a) Overview of voltage (AC to GND) measurement result (half period)



(b) Zoomed in (x-axis) to show three pulses of the measurement results

Figure 19: Simulation results from three phase operation featuring the voltage from AC to ground using the Default Case, grounded heatsink. The frequency of visible oscillations in figure 19b is 625 kHz.

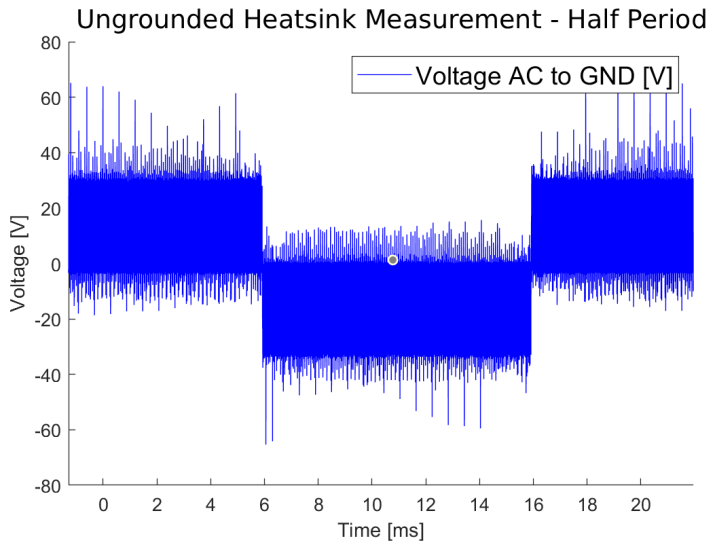
From figures 19b and 18b, the oscillation frequency is extracted. The frequencies are shown in Table 4.

Table 4: Grounded heatsink measurements and simulations with different configurations.

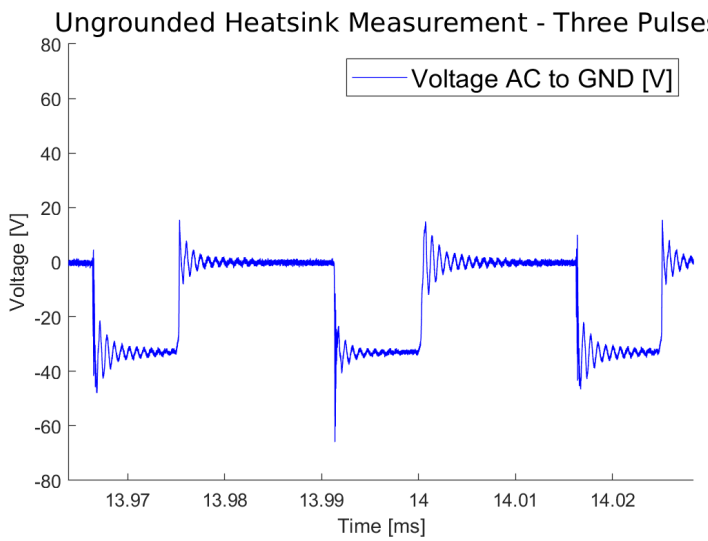
Grounded Converter Heatsink (Lower Freq.)	**Meas.**	**Sim.**	**ΔM**	**ΔS**	**S vs M**
	(MHz)	**(MHz)**	(%)	(%)	(%)
Default case	0.667	0.625	0.00	0.00	-6.30
Double line filter inductance	0.454	0.443	-31.93	-29.12	-2.42
Half line filter inductance	0.881	0.874	32.08	39.84	-0.79
1 nF parallel w/ IGBT (DC+)	0.645	0.612	-3.30	-2.08	-5.12
1 nF parallel w/ IGBT (DC-)	0.645	0.612	-3.30	-2.08	-5.12
1 nF parallel w/ C_DC+	0.465	0.517	-30.28	-17.28	11.18
1 nF parallel w/ C_DC-	0.515	0.513	-22.79	-17.92	-0.39
100 nF snubbers (DC+/-)	0.667	0.628	0.00	0.48	-5.85

Legend:
ΔM: Deviation of Measurement from Default Case Meas.
ΔS: Deviation of Simulation from Default Case Sim.
S vs M: Percentage difference between Simulation and Measurement.

The ungrounded heatsink case results are also shown in the same way as the grounded heatsink case.

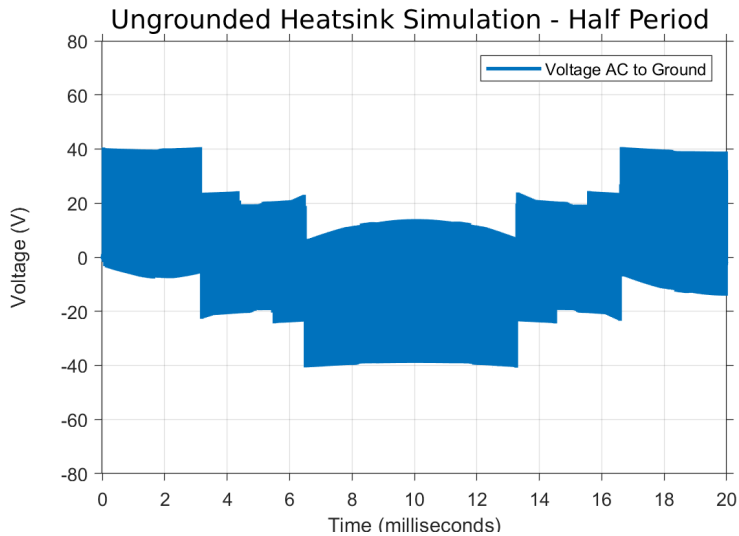


(a) Overview of voltage (AC to GND) measurement result (half period)

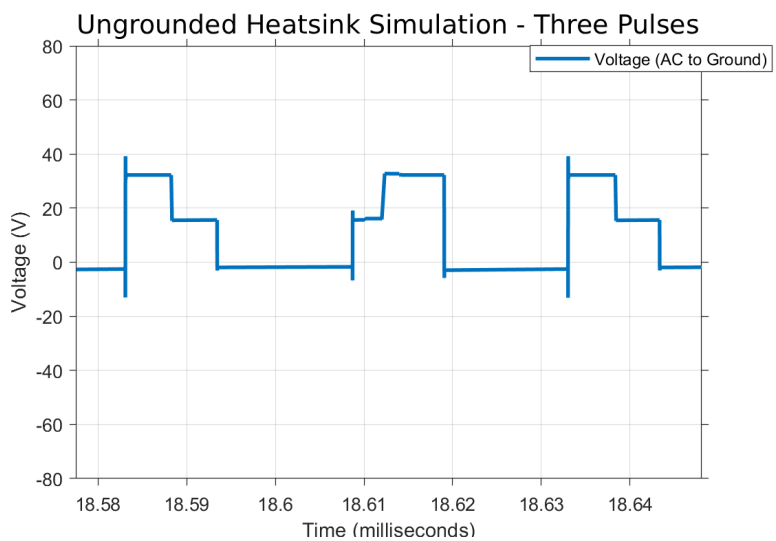


(b) Zoomed in (x-axis) to show three pulses of the measurement results

Figure 20: Measurement results from three phase operation featuring the voltage from AC to ground using the Default Case, ungrounded heatsink. The visible frequency of oscillations in figure 20b is 1.35 MHz



(a) Overview of voltage (AC to GND) measurement result (half period)



(b) Zoomed in (x-axis) to show three pulses of the measurement results

Figure 21: Simulation results from three phase operation featuring the voltage from AC to ground using the Default Case, ungrounded heatsink

Oscillations in the frequency range 0.6-1.8 MHz are present in the measurement (Figure 20b) but not in the simulation (Figure 21b)

Table 5: Ungrounded heatsink measurements and simulations with different configurations

Ungrounded Converter Heatsink (Lower Freq.)	**Meas. (MHz)**	**Sim. (MHz)**	**ΔM (%)**	**ΔS (%)**	**S vs M (%)**
Default case	1.35	not observed	0.00	N/A	N/A
Double line filter inductance	1.00	not observed	-25.93	N/A	N/A
Half line filter inductance	1.80	not observed	33.33	N/A	N/A
100 nF snubbers (DC+/-)	1.38	not observed	2.22	N/A	N/A

Legend:

ΔM: Deviation of Measurement from Default Case Meas.

ΔS: Deviation of Simulation from Default Case Sim.

S vs M: Percentage difference between Simulation and Measurement.

4.2.2. Higher frequency range oscillations (tens of MHz)

Higher frequency oscillations from the simulation and measurement are plotted. These higher frequency are found by zooming in further at the voltages (AC to GND) when they switch voltage levels, as is found in figures 22 and 23.

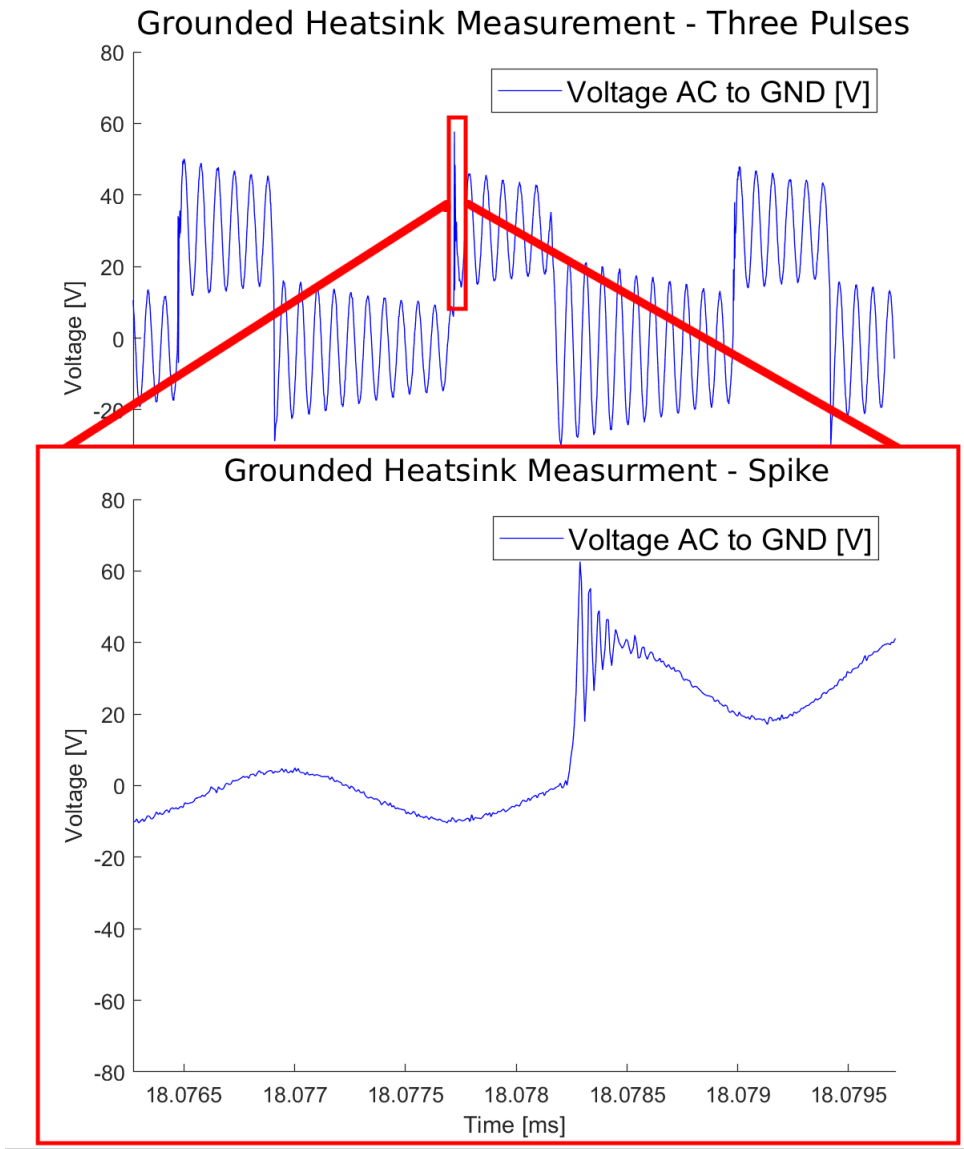


Figure 22: Higher frequency oscillations found in grounded heatsink measurements

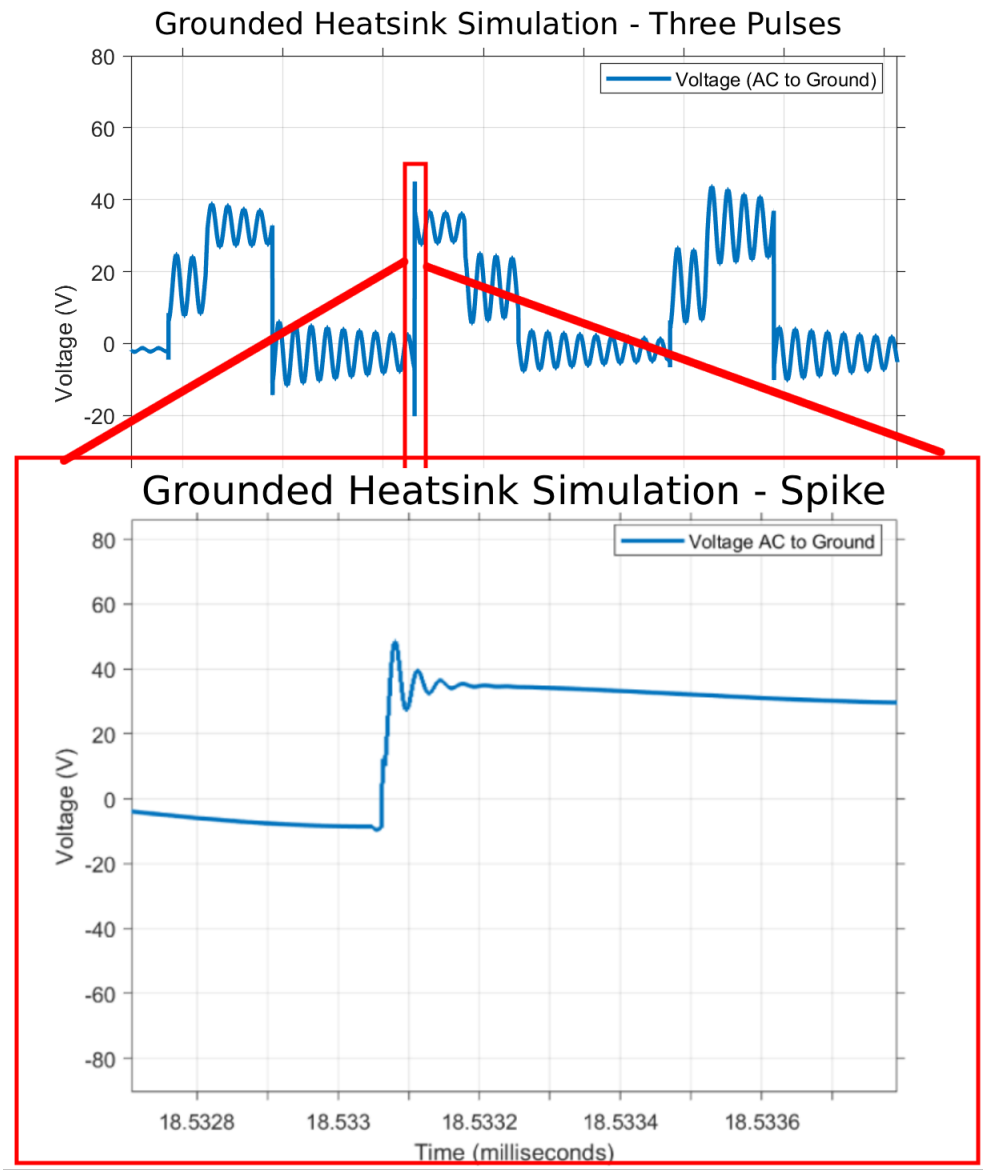


Figure 23: Higher frequency oscillations found in grounded heatsink simulations

Table 6: Higher frequency oscillations from grounded heatsink simulations and measurements

Grounded Converter Heatsink (Higher Freq.)	**Meas. (MHz)**	**Sim. (MHz)**	**ΔM (%)**	**ΔS (%)**	**S vs M (%)**
Default case	20.80	31.57	0.00	0.00	51.78
Double line filter inductance	20.86	31.49	0.29	-0.25	50.96
Half line filter inductance	20.85	31.50	0.24	-0.21	51.08
1 nF parallel w/ IGBT (DC+)	19.50	28.87	-6.25	-8.57	48.05
1 nF parallel w/ IGBT (DC-)	19.01	28.07	-8.61	-11.09	47.66
1 nF parallel w/ C_DC+	20.80	31.50	0.00	-0.22	51.44
1 nF parallel w/ C_DC-	20.80	31.50	0.00	-0.22	51.44
100 nF snubbers (DC+/-)	20.90	31.57	0.48	0.00	51.05
Doubling L-DClink inductances	N/A	24.20	N/A	-23.34	N/A

Legend:
ΔM: Deviation of Measurement from Default Case Meas.
ΔS: Deviation of Simulation from Default Case Sim.
S vs M: Percentage difference between Simulation and Measurement.

Investigating these higher frequencies (tens of MHz) with the converter heatsink ungrounded yields almost the same results, which is seen in figures 24, 25 and Table 7

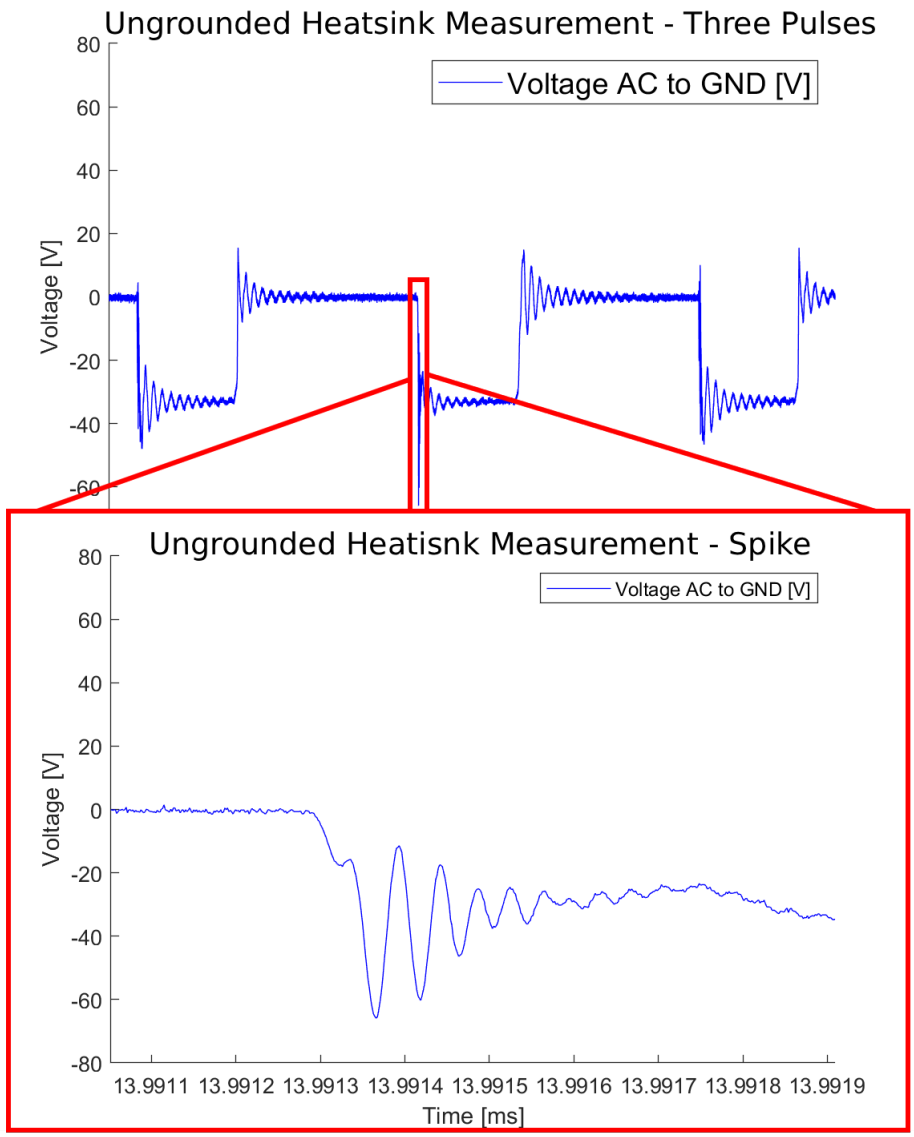


Figure 24: Higher frequency oscillations found in grounded heatsink measurements

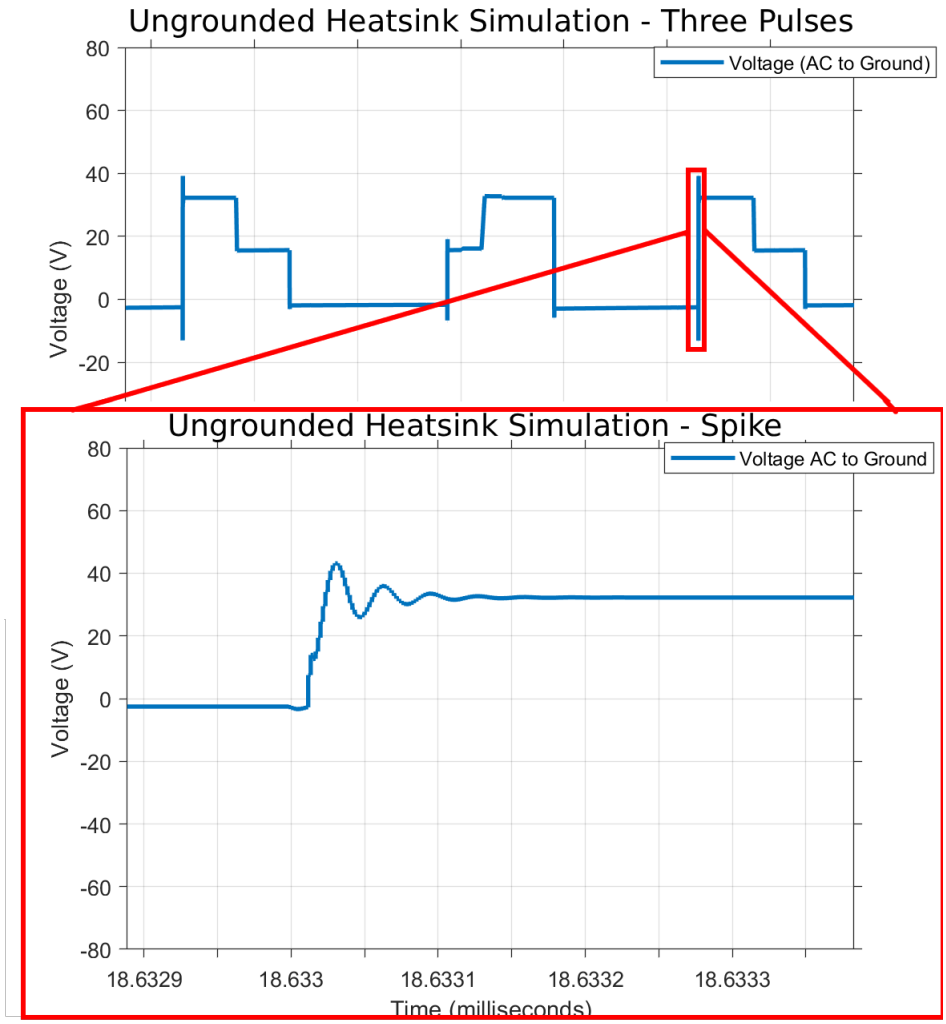


Figure 25: Higher frequency oscillations found in grounded heatsink simulations

Table 7: Higher frequency oscillations from ungrounded heatsink simulations and measurements

Ungrounded Converter Heatsink (Higher Freq.)	**Meas.**	**Sim.**	**ΔM**	**ΔS**	**S vs M**
	(MHz)	**(MHz)**	**(%)**	**(%)**	**(%)**
Default case	21.50	31.57	0.00	0.00	46.84
Series line filter Inductors	21.50	31.49	0.00	-0.25	46.47
Parallel line filter Inductors	21.50	31.50	0.00	-0.21	46.51
1 nF parallel w/ IGBT (DC+)	19.32	28.87	-10.14	-8.57	49.43
1 nF parallel w/ IGBT (DC-)	18.98	28.07	-11.72	-11.09	47.90
1 nF parallel w/ C_{DC+}	21.40	31.50	-0.47	-0.22	47.20
1 nF parallel w/ C_{DC-}	21.50	31.50	0.00	-0.22	46.51
100 nF DC terminals snubber	21.50	31.57	0.00	0.00	46.84
Doubling L-DClink inductances	N/A	24.20	N/A	-23.34	N/A

Legend:
ΔM: Deviation of Measurement from Default Case Meas.
ΔS: Deviation of Simulation from Default Case Sim.
S vs M: Percentage difference between Simulation and Measurement.

Doubling the L-DClink inductances was not feasible in measurements which is why it is not available in tables 6 and 7.

4.3. Double pulse test

DPT using measurement and simulation results are presented. First, the plots of the measurements and simulations are shown, then the oscillation frequencies are tabled. The oscillations frequencies investigated are in the tens of MHz range and not the lower frequencies despite them being present. The reason for leaving out the lower frequencies in the DPTs is because they are in the range 300-400 kHz.

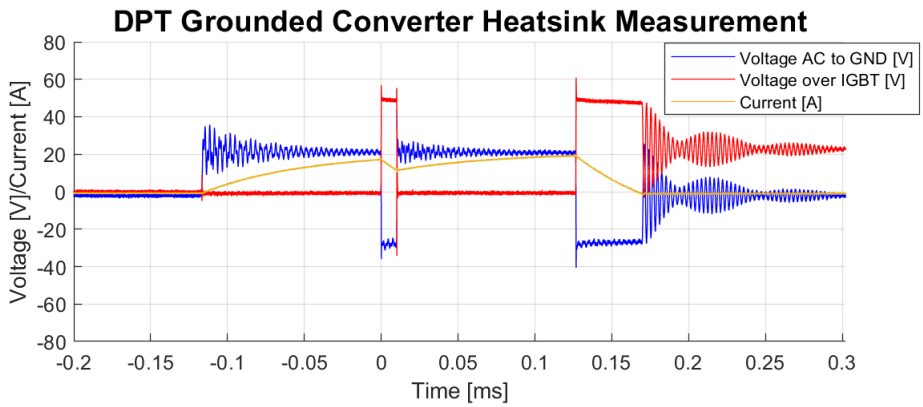


Figure 26: DPT measurement results for grounded heatsink configuration

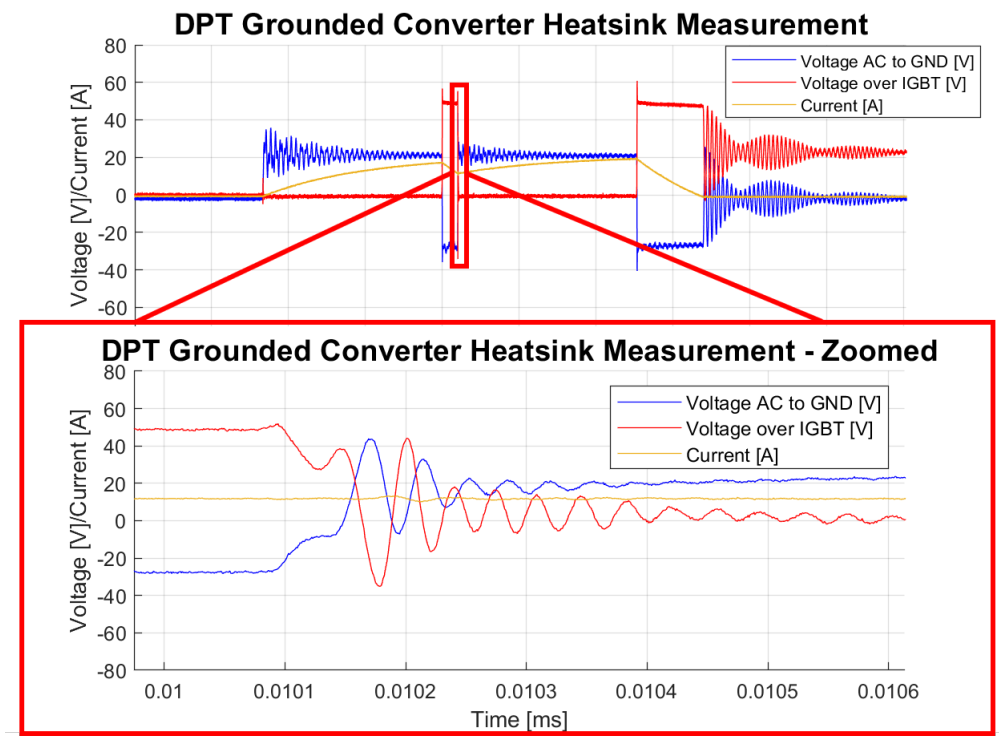


Figure 27: DPT measurement results using a grounded converter heatsink. The figure is zoomed in the x-axis so that an oscillations frequency is visible

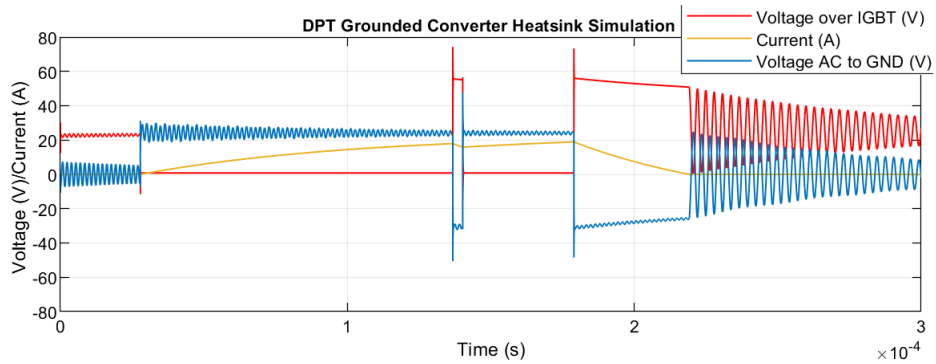


Figure 28: DPT simulation results for grounded heatsink configuration

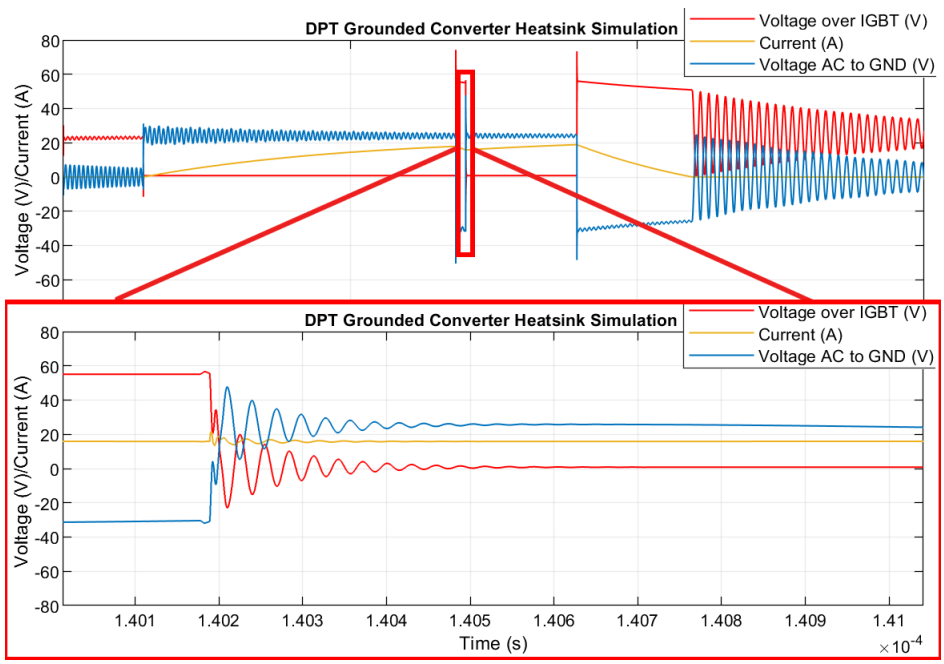


Figure 29: DPT simulation results for grounded heatsink configuration. The figure is zoomed in the x-axis so that an oscillations frequency is visible

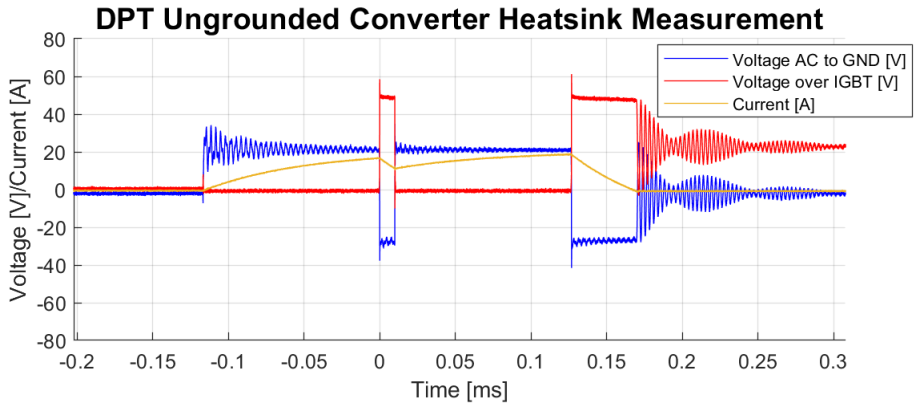


Figure 30: DPT measurement results grounded heatsink configuration

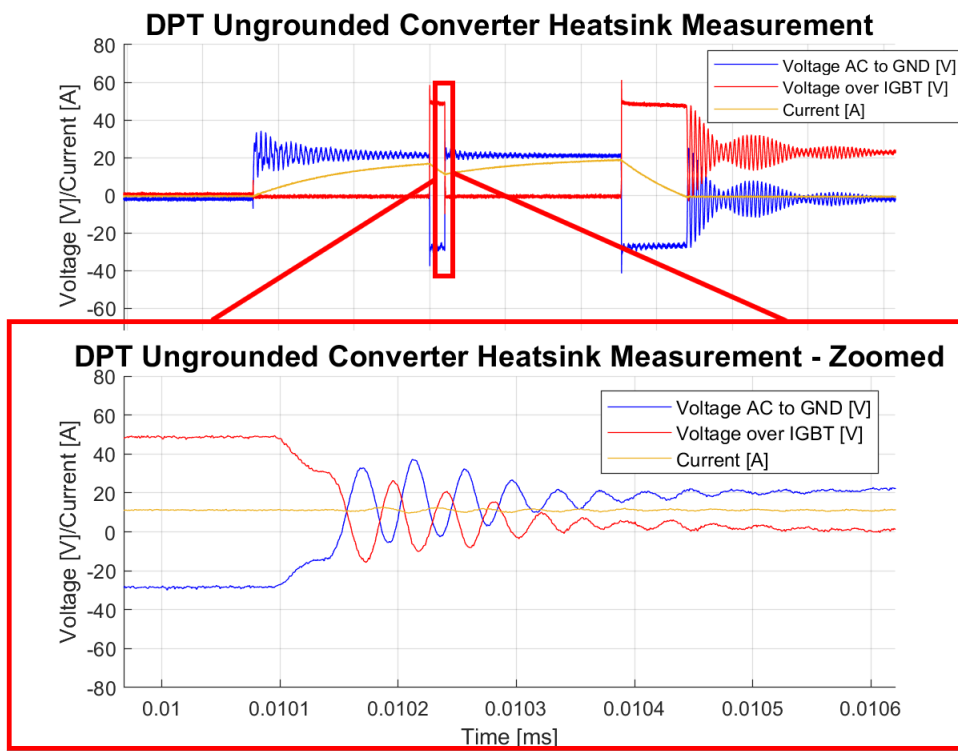


Figure 31: DPT measurement results using an ungrounded converter heatsink. The figure is zoomed in the x-axis so that an oscillations frequency is visible

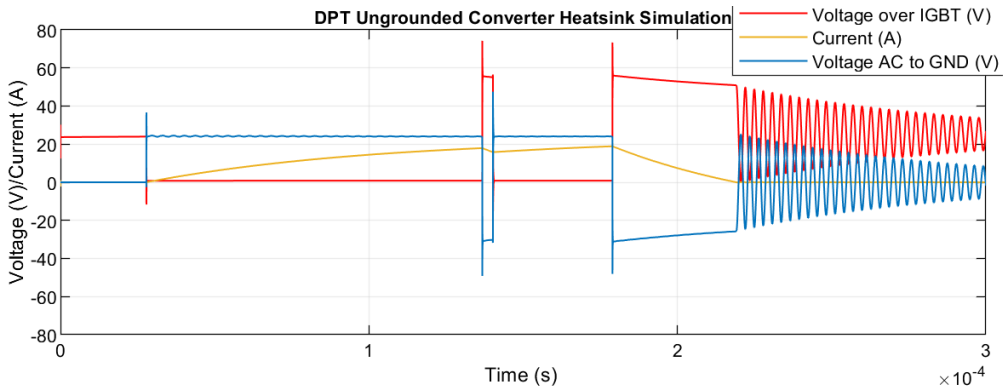


Figure 32: DPT Simulation results for ungrounded heatsink configuration

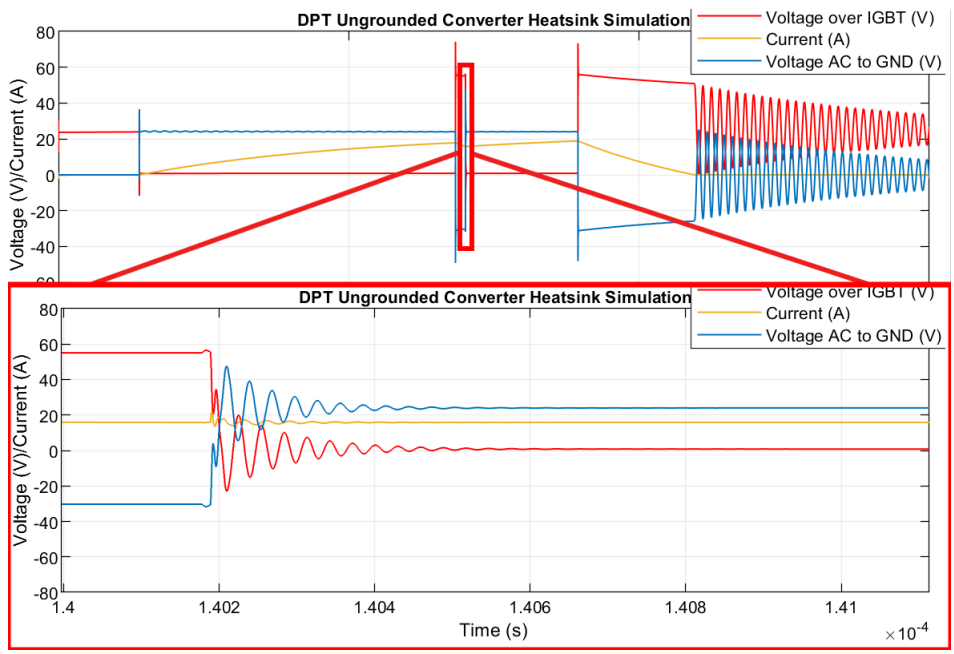


Figure 33: DPT simulation results for grounded heatsink configuration. The figure is zoomed in the x-axis so that an oscillations frequency is visible

Table 8: Comparison of Measurement and Simulation Frequencies for the Double Pulse tests

Double Pulse test	**Sim. (MHz)**	**Meas. (MHz)**	**ΔS (%)**	**ΔM (%)**	**S vs M (%)**
Grounded Heatsink	33.8	22.7–26.7	0.00	0.00	26.6–48.9
Ungrounded Heatsink	33.8	22.0–24.0	0.00	0.00	40.8–53.6
Doubled L-DClink inductances (Grounded)	22.0	N/A	-34.91	N/A	N/A
Doubled L-DClink inductances (Ungrounded)	22.0	N/A	-34.91	N/A	N/A

Legend:
ΔS: Deviation of Simulation from Default Case Sim.
ΔM: Deviation of Measurement from Default Case Meas.
S vs M: Percentage difference between Simulation and Measurement.

Note: Measurement ranges indicate frequency bands; S vs M computed using midpoint values.

Table 9: Comparison of Simulation Times using a Laptop with Intel Core i7-14700 HX processor and 16 GB RAM: Three Phase Operation vs. Double Pulse Test

Simulation Times	**Three Phase Operation (Minutes)**	**Double Pulse Test (Minutes)**	**Time Saved from DPT (Minutes)**
Test 1	63.5	3.3	60.2
Test 2	65.4	3.4	62
Test 3	67	3.2	63.8
Test 4	64.1	3.3	60.8
Test 5	58.4	3.3	55.1
Average	**63.7**	**3.3**	**60.4**

5. DISCUSSION

The primary objective of this thesis was to assess the feasibility of a model-based approach for predicting EMC performance during the design phase of converters like the ADF P25. The following sections interpret the findings in the context of high-frequency modeling, parasitic characterization, and the limitations of simulation environments.

5.1. Link inductance measurements

The reason the DC-link circuit has parasitic inductance is because any conductor conducting electricity inherently generates a magnetic field which creates and inductance (Semmlow, 2005). The reason the three values for parasitic inductances not being the same is because the current takes different paths for each of the phases with L2 being the shortest path meanwhile L3 is the longest which leads to inductance being the lowest for L2 and highest for L3. Link inductance measurements (Section 4.1, Figure 17, Table 3) provided practical values for the parasitic inductances of the DC-link capacitor board. The measured inductances per phase (DC+ to DC-) were 20.0 nH (L1, average), 16.4 nH (L2), and 18.0 nH (L3).

These values were implemented in simulation model by splitting each phase inductance into two (one for the positive DC rail and one for the negative DC rail). The use of average values (e.g., 10 nH per leg for L1) is a reasonable simplification given that the frequency dependence was small across the 100 kHz–15 MHz range. However, impedance analyzer measurements at very low impedances (a few mΩ) may introduce some error, as the instrument is optimized for 50 Ω loads. Nevertheless, the relative consistency across each phase supports the validity of the extracted values. In the future, new measurements can be

done by introducing a higher resistance in series in order to extract more accurate inductances from the DC-link capacitors.

These measured inductances were critical for improving the accuracy of the simulation model. Without them, the DC-link parasitic inductance would remain an unknown tuning parameter. The good match between grounded simulations and measurements in tables 4 - 8 suggests that the extracted inductance values are appropriate.

5.2. Current path oscillations

The results presented in Section 4.2 unequivocally demonstrate that the current path, and consequently the oscillatory behavior of the system, is fundamentally governed by the grounding configuration of the DUT heatsink. This aligns with the foundational theory of CM and DM EMI, which predicts that the presence or absence of a low-impedance path to ground will drastically alter the effective impedance of the resonant circuits. The experimental data provides substantial evidence for this mechanism.

When the heatsink is grounded, the measured oscillation frequency in the lower frequency range settles at 0.667 MHz (Table 4, Default Case). This configuration establishes a well-defined common-mode current path. As described in Section 2.3, common-mode currents flow in the same direction through the phase conductors and return via an unintended path, which in this case is the ground connection. The grounded heatsink provides a coupling path for the parasitic capacitances between the DC-link terminals and the heatsink (C_DCplus, C_DCminus, C_AC), which inserts them into the resonant loop. The result is a larger total effective capacitance in the circuit, which, according to the resonance formula $f = \frac{1}{2\pi\sqrt{LC}}$, lowers the resonant frequency. The simulation model for the grounded configuration reproduced this behavior with reasonable quantitative

accuracy, yielding a frequency of 0.625 MHz, a deviation of only -6.3% from the measurement.

In contrast, when the heatsink is ungrounded, the measured lower-frequency oscillation jumps to 1.35 MHz (Table 5) which is more than double the grounded case frequency. This shift is a direct consequence of a changed coupling path. Without a solid ground connection, the common-mode return path is severed. The noise currents are forced to return via poorly defined stray paths, which fundamentally changes the circuit's topology from predominantly common-mode to a more differential-mode or complex floating network. In this configuration, the parasitic heatsink capacitances are no longer referenced to ground, meaning they are either disconnected from the dominant resonant loop or configured in a series combination that presents a smaller effective capacitance. This smaller capacitance, in turn, produces a higher resonant frequency.

However, the simulation model failed to reproduce this 1.35 MHz oscillation (Table 5), revealing a critical gap in its fidelity for the ungrounded configuration. This failure occurs because the present model only includes parasitic capacitances that are referenced to ground—specifically C_DCplus, C_DCminus, and C_AC to the grounded heatsink. When the heatsink is left floating, the dominant resonant loop is formed by stray capacitances that do not involve a ground reference, such as phase-to-phase coupling, phase-to-DC-rail coupling, and distributed capacitances across the floating heatsink structure. These differential-mode and floating coupling paths were not characterized or included in the simulation model because they cannot be estimated from simple two-terminal impedance measurements; instead, they require extraction from 3D electromagnetic field simulations of the complete physical layout, or direct wideband impedance measurements between all relevant node pairs in the ungrounded configuration. In contrast, when the heatsink is ungrounded, the measured lower-frequency oscillation jumps to 1.35 MHz (Table 5) which is more than double the grounded

case frequency. This shift is a direct consequence of a changed coupling path. Without a solid ground connection, the common-mode return path is severed. The noise currents are forced to return via poorly defined stray paths, which fundamentally changes the circuit's topology from predominantly common-mode to a more differential-mode or complex floating network. In this configuration, the parasitic heatsink capacitances are no longer referenced to ground, meaning they are either disconnected from the dominant resonant loop or configured in a series combination that presents a smaller effective capacitance. This smaller capacitance produces a higher resonant frequency.

Beyond the layout-level coupling, the frequency-dependent behavior of the discrete components, such as the inductors, presents another layer of complexity, since real-world inductors exhibit parasitic effects, such as inter-winding capacitance and frequency-varying core losses, which lead to a self-resonant frequency. Although these were approximated in the current model using standard data, a more detailed characterization of the inductors' frequency response would be necessary to fully capture the system's impedance profile at higher frequencies.

These findings directly addresses the first research question: how do different current coupling paths affect the current frequency spectrum? The answer is that they define it. The grounding configuration acts as a switch, toggling the system between a lower-frequency, capacitively-loaded common mode and a higher-frequency differential/floating mode, shifting the measured oscillation frequency by approximately 50%.

However, the quantitative accuracy of the simulation model diverges significantly for the ungrounded configuration. As shown in Table 5, the ungrounded simulation model completely fails to produce the 1.35 MHz oscillation seen in the measurements. This discrepancy highlights that while the model for the grounded CM path is relatively mature, the ungrounded model lacks key parasitic elements.

The range of lower frequency oscillations (600 kHz - 1.8 MHz) is not found in the simulations as there are no lower frequency oscillations. This means that the simulations should introduce a new coupling path for simulating the ungrounded heatsink properly. This suggests that accurately modeling a differential-mode EMI path requires a more granular, perhaps 3D electromagnetic field-based, extraction of stray capacitances than what was available for this thesis. The model, in its current state, can qualitatively predict that a frequency shift will occur, but cannot quantitatively predict the exact frequency in the ungrounded mode, placing it as a useful but not yet fully predictive tool for all configurations.

It should be noted that all measurements and simulations in this thesis were conducted at a DC-link voltage of 48 V, which is considerably lower than the converter's maximum rating of 415 V (phase-to-phase). Some parasitic capacitances in the system are voltage-dependent, meaning their values may change under higher operating voltages. Therefore, the quantitative results presented here may differ at higher voltages. The qualitative findings, such as dominant coupling paths and relative sensitivity trends, are expected to remain valid.

5.3. Dominant coupling paths

Identifying the dominant coupling paths is essential for a proactive model-based EMC design approach, as it tells engineers where to focus their mitigation and modeling efforts. The sensitivity analysis conducted in this thesis, particularly the parallel capacitor tests, provides a clear experimental method to answer the second research question: what are the main coupling paths for the system? The findings reveal a frequency-dependent hierarchy of dominant parasitic elements that directly aligns with the grounding configuration discussed in Section 5.2.

For the lower frequency range oscillations (600 kHz – 1.8 MHz) in the grounded heatsink configuration, the dominant common-mode coupling path is defined as

a conductive loop. This loop originates at the switching node (the AC output), couples through the parasitic capacitance between the transistor tab and the grounded heatsink, flows through the ground plane to the DC input terminals, and finally returns to the source via the parasitic capacitance between the DC bus and ground. The physical area enclosed by this loop, in combination with the high dv/dt of the switching node, dictates the magnitude of the coupled common-mode current. The experimental evidence for this is conclusive. By adding a 1 nF capacitor in parallel with C_DCplus, the measured oscillation frequency was dramatically reduced from 0.667 MHz to 0.465 MHz, a massive shift of -30.28% (Table 1). A similar, but slightly less pronounced effect was observed when adding 1 nF to C_DCminus, shifting the frequency by -22.79% to 0.515 MHz. From this observation, it can also be inferred that adding the same 1 nF capacitors to C_AC would also have a similar effect since these capacitors are connected to the same ground.

This high sensitivity confirms that C_DCplus and C_DCminus and the line filter inductors (L_1 and L_2) are not merely present but are the dominant reactive elements defining the fundamental resonant frequency of the common-mode current loop. The further sensitivity to line filter inductance configurations, which means that, with series inductance lowering frequency by -31.93% and parallel inductance increasing it by 32.08%-completes the picture of the dominant resonant tank: the primary loop consists of the line filter inductors (L) and the grounded heatsink parasitic capacitances (C). The fact that simulations (ΔS) mirrored these trends for both inductance and capacitance changes solidifies this conclusion.

In contrast, the addition of 100 nF snubber capacitors across the DC-link terminals had a negligible effect on the oscillation frequency, which remained at 0.667 MHz in both measurements. This is a critical and highly practical finding. It demonstrates that the high-frequency common-mode displacement current

does not flow through the external DC-link decoupling capacitors, but instead, it finds a lower-impedance path directly through the tightly coupled parasitic capacitances from the DC bus to the heatsink. From an EMC design perspective, this means that simply adding a larger external capacitor on the DC link is an ineffective strategy for mitigating these conducted emissions, as the dominant path is intrinsic to the physical layout and semiconductor module packaging.

The dominant coupling path shifts entirely for the higher frequency range oscillations (tens of MHz), regardless of the grounding configuration. In this domain, the sensitivity analysis points to the parasitic inductances of the DC-link and the IGBTs themselves as the primary components. As shown in Tables 3 and 4, varying the line filter inductance or the heatsink capacitances had no impact on the $\tilde{3}$1.57 MHz simulated or $\tilde{2}$0.8-21.5 MHz measured oscillation. However, adding 1 nF in parallel with the IGBT's output capacitance (DC+ or DC-) caused a reduction in this high-frequency oscillation (e.g., an -8.57% shift in simulation), while doubling the DC-link inductances in the simulation caused a dramatic -23.34% frequency drop. This confirms a new dominant LC loop has emerged, one that bypasses the larger line filter inductor components and oscillates locally between the DC-link busbar inductances and the semiconductor's parasitic junction capacitances.

The mismatch between the simulation (31.57 MHz) and measurement ($\tilde{2}$1.5 MHz) in this range, which was significantly reduced by scaling the DC-link inductance, strongly suggests that the true physical inductance in this path is larger than what was measured on the DC link PCB alone. This points to a dominant coupling path that includes unmodeled internal inductances within the IGBT package itself which is a key parasitic that must be accounted for in future model developments to increase model accuracy.

5.4. *Stray component parameters' influence the frequency content in the output current (Sensitivity Analysis)*

The sensitivity analysis conducted through systematic parameter variation reveals a clear frequency-dependent hierarchy of dominant parasitic elements. The finding of utmost importance is that modifying the parasitic capacitances between the IGBT terminals and the DC-link inductances predominantly affects the higher-frequency oscillations (tens of MHz), while the converter heatsink capacitances and line filter inductances govern the lower-frequency oscillations (600 kHz – 1.38 MHz). This division is not arbitrary but stems from the distinct resonant loops formed at different frequency ranges, as illustrated in Figure 34

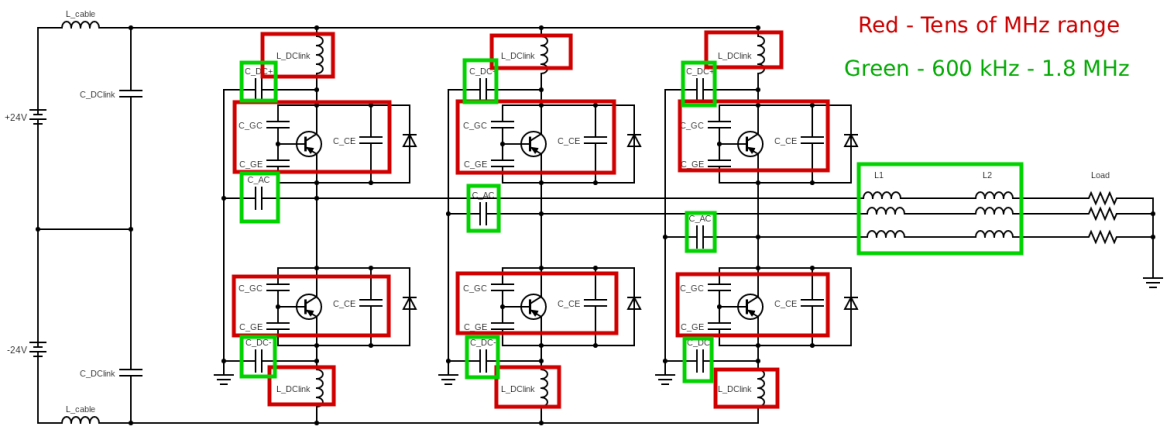


Figure 34: Circuit diagram of the DUT with parasitic capacitance present. The circuit has been marked to highlight which frequency the electrical components are responsible for.

In Table 4 it is seen that the default case exhibits a measured oscillation frequency of 0.667 MHz and a simulated frequency of 0.625 Mhz which represents a simulation-to-measurement deviation of 6.3%. Adding 1 nF capacitors in parallel with the IGBTs at the DC+ or DC- sides produced minor shifts in lower frequency oscillations with the measured frequency decreased by 3.30% to 0.645 MHz, while the simulated frequency changed by 2.08% to 0.612 MHz. In contrast, the same 1 nF addition significantly impacted the higher-frequency oscillations shown in

Table 6, where the simulated frequency dropped from 31.57 MHz to 28.87 MHz (DC+ case, 8.57%) and the measured frequency decreased from 20.80 MHz to 19.50 MHz (6.25%), since adding 1 nF in parallel with the IGBTs effectively doubles the IGBT capacitance from the collector to emitter terminals which can be seen in Table 2. Doubling the DC-link inductances produced an even more dramatic effect in the higher-frequency range, reducing the simulated frequency by 23.34% from 31.57 MHz to 24.20 MHz, while leaving the lower-frequency oscillation essentially unchanged.

The lower-frequency range, by contrast, proved highly sensitive to the converter heatsink parasitic capacitances C_DCplus and C_DCminus. According to Table 1, adding 1 nF parallel to C_DCplus reduced the measured frequency by 30.28% from 0.667 MHz to 0.465 MHz, and adding 1 nF parallel to C_DCminus reduced it by 22.79% to 0.515 MHz. The line filter inductor configuration also demonstrated substantial influence on the lower-frequency oscillation, since doubling the inductance decreased the measured frequency by 31.93% to 0.454 MHz, while reducing the inductance by half increased it by 32.08% to 0.881 MHz. Table 5 confirms that these trends hold for the ungrounded configuration as well, with series inductance reducing the measured frequency by 25.93% and parallel inductance increasing it by 33.33%. The simulations for 5 can't be applied here since there are no such oscillations in for the ungrounded simulations for three phase operation.

The 100 nF capacitor placed across the DC terminals had no effect on both frequency ranges. This is seen first in Table 4 there the measured frequency remained as 0.667 MHz. Then in Table 6 there was only a slight deviation from 20.80 MHz to 20.90 MHz (+0.48%). This pattern also holds for the corresponding simulations. This finding carries external implications, which is that external decoupling capacitors, while essential for power quality, do not substantially alter the high-frequency resonant paths responsible for conducted EMI. The parasitic

elements intrinsic to the converter layout and semiconductor packaging dominate the EMI behavior.

These findings show that traditional decoupling strategies are ineffective for conducted EMI; instead, engineers must minimise parasitic capacitances to the heatsink and bond-wire inductances at the design stage. However, while such source-level mitigation minimizes the noise injected into the system, capacitors must still be added to the line filter inductors to form an LCL topology. This is not for traditional decoupling, but to define and minimize the unavoidable common-mode coupling loop between the converter, its DC power source, and the external environment, thereby preventing the remaining high-frequency noise from radiating on the DC cable harness.

5.5. Double pulse test

The main purpose of the DPT is to obtain the same results while significantly reducing the simulation time. As shown in Table 9, the DPT reduced the simulation time by up to 95% while still producing nearly identical signal behavior in terms of high frequency oscillations. For every planned or unplanned modification to the normal operation model, the changes should first be implemented and tested on the DPT model due to its faster simulation performances, since in the real world, reducing simulation time from over an hour to three minutes allows a designer to evaluate dozens of layout variants in a single afternoon, enabling true model-based EMC optimisation. The implemented changes should thereafter be transferred to the continuously operating model to verify and validate the results under normal operating conditions.

Comparing the results from the continuous operation model in Table 6 and DPT in table 8 for the grounded heatsink case, it can be observed that the results are relatively close. This indicates that the DPT model has fulfilled its purpose of reproducing measurement results while maintaining shorter simulation times.

For the DPT model, the simulated resonance frequency was 33.8 MHz, while the measured resonance frequency was between 22.7 MHz and 26.7 MHz. For the continuously operating model, the simulated resonance frequency in the default case was 31.57 MHz, whereas the measured resonance frequency was 20.8 MHz. The ungrounded heatsink results from both the continuously operating model and the DPT model also showed similar behavior.

In Table 8, the last column represents the case where the DC-link inductance was doubled. This modification was made because the hypothesis was that the DC-link inductance together with the IGBT capacitances are mainly responsible for the high-frequency resonance. Since the measured resonance frequency shown in the same table is lower than the simulated one, it was assumed that some inductive effects were not fully represented in the simulation model. By doubling the DC-link inductance, the simulation results became closer to the measured results. This modification was first implemented and tested on the DPT model due to its faster simulation time, and was later transferred to the continuously operating model where similar results were observed.

5.6. Thesis objectives

1. How do different current coupling paths and stray components affect the dominant oscillation frequency? The measured dominant ringing frequency is strongly dependent on the grounding configuration of the converter heatsink. Grounding the heatsink creates a dominant common-mode path through ground, which inserts parasitic heatsink capacitances into the resonant loop, increasing the effective capacitance and lowering the resonant frequency (measured: 0.667 MHz; simulated: 0.625 MHz). In the ungrounded configuration, the defined common-mode return path is severed, forcing noise currents into differential-mode or floating stray paths. This raises the measured lower-frequency oscillation to 1.35 MHz which is more than double the grounded case frequency. The un-

grounded simulation model failed to produce this 1.35 MHz oscillation, indicating that present models lack key parasitic elements for differential-mode coupling paths. It should be noted that these frequencies were identified from time-domain waveforms; full spectral measurements (FFT) were not available and would be valuable in future work to determine whether additional significant frequency components exist beyond the dominant oscillation reported here."

2. What are the main coupling paths for the system? The main coupling paths are the parasitic capacitances between the AC output and the DC terminals, specifically those referenced to ground through the heatsink. Adding 1 nF in parallel with C_DCplus reduced the measured lower-frequency oscillation from 0.667 MHz to 0.465 MHz (-30.28%), and adding 1nF to C_DCminus reduced it to 0.515 MHz (-22.79%). By contrast, adding 100 nF snubber capacitors across the DC terminals had no measurable effect (frequency remained at 0.667 MHz), proving that external DC-link decoupling capacitors do not alter the low-frequency resonant paths responsible for conducted EMI. For higher-frequency oscillations (tens of MHz), the dominant coupling paths shift to parasitic inductances of the DC-link and the IGBT package itself.

3. How do stray component parameters influence the frequency content in the output current? The output current's frequency content exhibits a clear frequency-dependent hierarchy of sensitivity.

Lower frequencies (600 kHz – 1.8 MHz): Highly sensitive to heatsink parasitic capacitances and line filter inductors. Doubling line filter inductance decreased the measured frequency by 31.93% (to 0.454 MHz), while halfing line filter inductance increased it by 32.08% (to 0.881 MHz).

Higher frequencies (tens of MHz): Sensitive to DC-link and IGBT parasitic inductances. Doubling the DC-link inductances in simulation reduced the high-frequency oscillation by 23.34% (from 31.57 MHz to 24.2 MHz), bringing the simulation significantly closer to the measured value (20.8–21.5 MHz).

Adding 1 nF in parallel with the IGBT's DC+ terminal reduced the simulated high-frequency oscillation by 8.57% (to 28.87 MHz).

Insensitive parameters: The 100 nF snubber that was connected between DC + and DC - across each leg, changed the measured high-frequency oscillation by only +0.48% (from 20.80 to 20.90 MHz), confirming that external decoupling capacitors do not mitigate conducted EMI from intrinsic parasitic elements.

These results demonstrate that standard power flow models, which ignore layout-dependent parasitics, cannot capture conducted EMI behavior. Proactive model-based EMC requires experimental characterization of heatsink capacitances, line filter inductors, DC-link parasitic inductances, and, critically, the internal inductances of the IGBT package itself.

5.7. Design guidlines for EMC in power electronic converters

Based on the sensitivity analysis and validation results presented in this chapter, the following practical guidelines are recommended for engineers performing model-based EMC analysis of IGBT-based voltage source converters:

Grounding strategy: Grounding the converter heatsink establishes a predictable common-mode path that the simulation model can capture with reasonable accuracy (deviation $<10\%$), while ungrounded configurations produce higher-frequency oscillations but require 3D-extracted stray capacitances for quantitative prediction. In early design phases where simulation fidelity is paramount, a grounded heatsink configuration is recommended.

Busbar layout: The high-frequency oscillation (tens of MHz) is dominated by parasitic inductances in the DC-link and IGBT package. Minimising the physical loop area of the DC-link busbar directly reduces this parasitic inductance and shifts the resonance to higher, potentially less harmful frequencies. However,

high frequencies can increase the risk of emissions, but the amplitude may also decrease, which is equally beneficial.

Decoupling capacitor strategy: External DC-link snubber capacitors (100 nF) showed negligible effect on both low- and high-frequency conducted emissions. Mitigation efforts should instead focus on minimising the intrinsic parasitic capacitances from the DC-link terminals to the heatsink, and on optimising the line filter inductor design.

Accelerated EMC screening: The DPT excites the same resonant frequencies as continuous three-phase operation while reducing simulation time from over 60 minutes to approximately 3 minutes. This enables rapid evaluation of layout changes, component substitutions, and parasitic variations during the design phase.

6. CONCLUSION

This thesis demonstrated a model-based EMC (MB-EMC) workflow for an IGBT-based voltage source converter, focusing on conducted emissions in the 150 kHz to tens of MHz range. The primary conclusion is that a validated simulation model, when parameterized with accurate layout-dependent parasitic elements, can qualitatively and, in specific configurations, quantitatively predict the oscillatory noise behavior that may lead to EMI.

The investigation confirmed that the grounding configuration of the converter is the single most influential factor on the noise spectrum, acting as a switch between common-mode and differential-mode dominant current paths. Through a systematic sensitivity analysis, this work identified the parasitic capacitances from the DC-link to the grounded heatsink and line filter inductors as the dominant coupling path for lower-frequency oscillations, a finding experimentally validated through targeted impedance modifications.

For higher-frequency oscillations in the tens of MHz range, the study revealed that parasitic inductances both from the DC-link layout and the internal IGBT package are the dominant parameters. Doubling the modeled DC-link inductances to implicitly account for unmodeled IGBT internal inductances shifted the simulated high-frequency resonance from 31.57 MHz to 24.2 MHz which is significantly closer to the measured value of 20.8/21.5 MHz. This finding underscores that achieving quantitative accuracy at high frequencies requires modeling not just the printed circuit board and busbar parasitics, but also the inductive parasitics inherent to the semiconductor modules themselves.

The DPT was shown to be a viable method for accelerating the simulation-based part of the MB-EMC workflow, as it excites the same resonant dynamics as continuous operation in a fraction of the simulation time. Ultimately, this thesis

provides a robust framework for bridging the gap between theoretical simulation and physical EMC measurements, enabling proactive EMC analysis during the design phase of power electronic converters.

6.1. Future research

To further advance this MB-EMC methodology, future work should focus on three areas. First, a detailed extraction and modeling of the stray capacitances in the ungrounded configuration is necessary to achieve quantitative simulation accuracy for that mode, potentially using 3D electric field solvers. This study demonstrated that these unmodeled capacitances are the likely cause of the discrepancy between the initial simulation and measurement results for the tens of MHz oscillation. Direct measurement or characterization using an impedance analyzer on a decapsulated or specially designed test module would allow these values to be integrated into the simulation model directly, rather than being accounted for implicitly by scaling the DC-link inductance.

Second, a detailed extraction and modeling of the stray capacitances in the ungrounded configuration is necessary to achieve quantitative simulation accuracy for that mode, potentially using 3D electric field solvers. Third, once the IGBT package parasitics are fully characterized, the validated model could be used to explore and pre-evaluate the impact of various EMI mitigation techniques, such as optimized busbar layouts, integrated EMI filters, and advanced gate-driving strategies, thereby fully realizing the proactive potential of model-based EMC.

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Appendix

A. Simulink Model

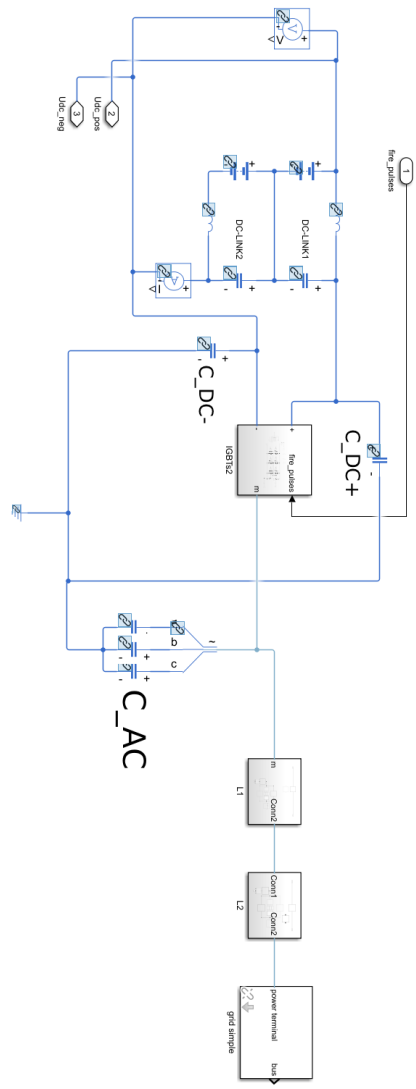

Figure 35: Simulink model setup. This model is used for both three phase operation and double pulse tests

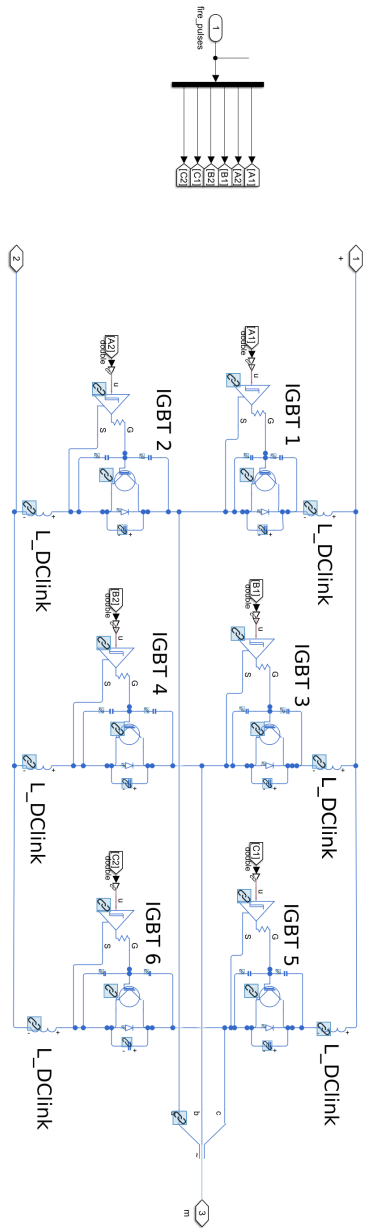

Figure 36: Simulink IGBT circuit model where the parasitic inductances are moved to the three phase voltage source converter.