Direct RF sampling ADC analog front-end for 6G

Olof Andréasson
ol1808an-s@student.lth.se
Theodor Callmar
th2374ca-s@student.lth.se

Department of Electrical and Information Technology
Lund University

Supervisor: Markus Törmänen
(EIT)

Company Supervisor: Per-Olof Brandt
(BeammWave)

Examiner: Pietro Andreani
(EIT)

June 17, 2026

Printed in Sweden
Tryckeriet i E-huset, Lund

Abstract

A time-interleaved ADC analog front-end is presented with a sampling rate of $64GS/s$. It has a hierarchical architecture of 2-4-4 giving 32 separate channels. Each channel is constructed by an input buffer, 1^{st} rank (T/H), sub-buffer, and 2^{nd} rank T/H. The complimentary clocking generation consist of a $32GHz$ differential signal divided down using a CML divide-by-4 and DFF divide-by-4 architecture. The required duty cycles for the time-interleaved network were generated using gate logic. The SFDR and SNR ranges from $41dBc$-$34dBc$ and $38dB$-$31dB$ respectively within the FR3 band. In stable state, the total power consumption of the analog front-end is $484mW$ including the interleaving network and clock generation. This was constructed using GlobalFoundaries 22FDX technology node. All simulations were done in Cadence Virtuoso environment.

Popular Science Summary

All modern mobile phones and other electronic equipment that utilize wireless communication needs to have a receiving and transmitting architecture. These architectures are built on many different components that together makes wireless communication possible. As the speed of the communication increases with newer standards, as with 5G NR and the coming 6G, more reliable and speedy components have to be made.

The standards for 5G NR and 6G has enabled higher data-rate communication, this is because newer frequency bands have become commercially open for use. These newly opened frequency bands are called FR2 and FR3, which include parts of the spectrum that are called centimeter- and millimeter-wave. These frequency band are upwards of tens of GHz where the used modulation bands increase in bandwidth compare to older standards.

These higher frequency signals also suffer from higher isotropic path loss. Meaning that the wireless signal has a very short range before it attenuates fully. A solution to this is to implement a technique called beamforming. The technique builds on several antenna modules working in unison to increase directivity and therefore gain.

Once the signal has been received by the beamforming antenna modules, it is directed to the receiving architecture. Older receiving architectures utilize a technique called down-mixing. This builds on converting higher frequency signals to a more manageable frequency. The state of the art research points to a new architecture called direct RF sampling. Older architectures include several stages to the analog front-end. With direct RF sampling, this front-end can be replaced by one larger network, which grants higher flexibility and supposedly lower power consumption.

In both architectures the end stage converts the analog RF signal to a digital representation. That conversion is done with the help of an analog-to-digital converter (ADC). The peak frequency that can be accurately converted to a digital representation is limited by the sample rate of the ADC. Higher sample rate ADC gives the possibility for higher input frequency signals to be converted. It is not possible to do conversion in the intended FR3 range using one single ADC, due to its limited sample rate. Thus to achieve the required sample rate for FR3 conversion many ADCs working in parallel

is needed. Each ADC receives a designated time-slot in which it alone is able to do a sample of the signal. In the next stage, on the digital side, all samples are combined to create the completed digital representation.

This Master's thesis will investigate the construction and implementation of a direct RF sampling architecture. This will be done in the technical transistor node of GlobalFoundaries 22FDX. Different design choices have been made and at the end of the thesis a complete analog front-end will be presented.

Table of Contents

List of Figures

Chapter 1
Introduction

The emerging 6G and existing 5G technologies have made GB/s communication possible. With such high data rates, many high demanding technologies have become possible as connected cars, cloud computing, Augmented Reality and Virtual Reality etc. This GB/s communication is made possible by the use of the mmWave band that the 5G standard introduced, moving away from the congested sub-6GHz spectrum. However, these high frequency ranges suffer from high path loss. To solve this, a multiple-input multiple-output (MIMO) network is implemented. With multiple transmitting antennas, a technique called beamforming can be used. The beamforming technique increases gain, gives higher directivity, and allows for spatial multiplexing.

The increased gain and directivity combat the intrinsic high path loss that mmWave has, but spatial multiplexing allows for an added benefit. Spatial multiplexing means that the same base station can provide several users simultaneously. This is due to the effect of beamforming, where a signal can be transmitted in a specific direction in space. With the superposition principle, two signals can be combined, allowing for a higher downlink speed.

BeammWave AB is a deep-tech company with expertise in communication solutions, composed of a group of engineers and technical experts whose objective is to revolutionize the 5G and 6G space. The company is focused on fully digital beamforming communication, ranging from systems and algorithms to designing both digital and radio-frequency (RF) integrated circuits (ICs). The first generation of 5G devices implemented analog beamforming. This technique is slow, especially in adapting to movement resulting in dropped communication links, and it does not take full advantage of the mmWave spectrum efficiently. By instead performing beamforming digitally with a systems approach, where each antenna has its own transceiver chain and the beamforming is done in the digital baseband, BeammWave can reduce power consumption to be better than or on par with analog beamforming, with much better adaption time to changing radio channel conditions and spectrum efficiency[1].

1.1 Analog-to-Digital Converter

Analog-to-digital converters (ADCs) are systems used to convert analog signals to digital signals for a computer system. In the physical world, signals are continuous

and always changing. However, computer systems are built on a binary foundation, which means that all quantities depicted in a computer system are discrete values. This difference between the analog domain (the physical world) and the digital domain (the computer system) creates an obstacle. To solve this, one needs to use an ADC.

The ADC takes a sample of the signal at specific intervals, called the sampling rate, and it is given in units of samples per second, S/s. These samples are then combined in the digital domain to create a representation of the analog signal. The rate of the samples determine the highest signal frequency that can be perceived and represented correctly in the digital domain. This highest frequency that can be represented in the digital domain is called the Nyquist frequency of the ADC system. This frequency is determined from the Nyquist-Shannon Theorem[2], which says that to be able to represent a signal with the frequency f, one needs to have a sample rate of at least double the frequency of the signal, i.e., $2 \cdot f\ S/s$.

In the digital domain, signals are represented using discrete values, contrary to the analog domain where they are continuous. The resolution in the digital domain is represented by the number of bits the system has. For example, an ADC with a resolution of 6-bits has $2^6 = 64$ different discrete levels.

1.2 Time-Interleaved ADC

As modern communication technologies implement more advanced modulation techniques and higher carrier frequencies, in the tens of GHz, the need for higher sampling rate analog-to-digital converters are sought after. One technique is in the forefront for high sample rate ADCs and that is time-interleaved ADCs. Time-interleaved (TI) ADCs utilize several lower sampling rate sub-ADCs in parallel. By buffering the RF input signal to the sub-ADCs a higher sampling rate can be achieved, unlocking what before was thought to be impossible.

A TI ADC receives the analog signal and distributes it with its branching front-end to the sub-ADCs. Each sub-ADC receives one time interval of the analog signal that the sub-ADC then decodes to a digital representation of the input signal.

This time-interleaved distribution is thought to be a more viable option to the analog front-end (AFE) in today's receivers. Current receiver technology is called super-heterodyne. The received signal is down-converted to an intermediate frequency(IF) with the same characteristics as the RF signal, meaning the IF signal carries the information. This IF signal is then sent for decoding to the ADC. This receiving method has been the standard for decades. However, with a higher sampling rate, in the tens of GS/s, direct RF sampling is a possibility. This would change the RF receiving architecture and allow for a more flexible design.

1.3 Goal of Project

The goal of the project is to design and implement a schematic representation of a functioning TI ADC network. The design of the network is limited to the AFE and the clock generation of the system. The TI network should have a Nyquist frequency that encapsulates the frequency range 3 (FR3), 7.125GHz to 24.25GHz,

that will supposedly be part of the coming 6G standard. The focus in this thesis is on pushing the limits of GlobalFoundries 22FDX technology, i.e. how high can the sampling speed be increased for the specific ADC architecture.

Chapter 2

Radio Frequency Receiving Architectures

Radio frequency (RF) receivers are the link between the analog signal domain and the digital signal domain. An antenna receives the transmitted analog signal and then passes it onward to the RF IC. Traditional receiving architectures implement a structure called super-heterodyne [3], see Figure 2.1.

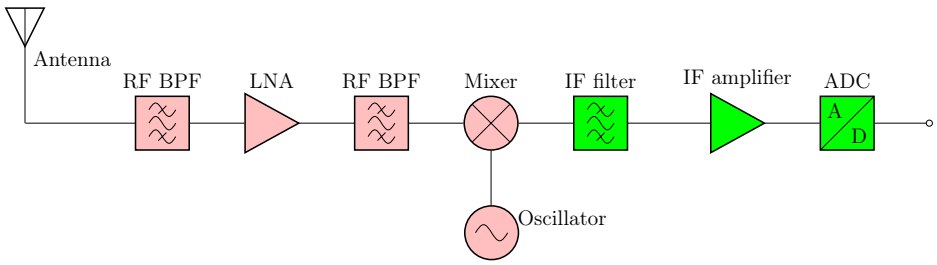

Figure 2.1: Super-heterodyne receiver. The pink color denotes RF domain and green color denotes IF domain.

The heterodyne structure converts the RF signal to an intermediate frequency (IF). This IF signal has a lower frequency that the analog-to-digital converter can sample. The down conversion of the signal is made to be able to convert the analog signal to a digital signal. It is the ADC's job to do the conversion, and to convert the signal properly, the IF signal must be within the first Nyquist zone of the ADC, see Figure 2.2.

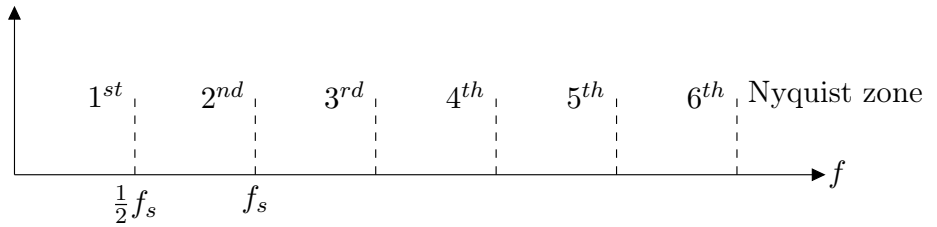

Figure 2.2: Nyquist zones.

This is to avoid aliasing. If the IF signal is outside the first Nyquist zone, the signal will be aliased into the 1^{st} Nyquist zone and be wrongly assumed to

be another signal. The RF signal, in the super-heterodyne case, is first filtered and then amplified by a low noise amplifier (LNA). It is filtered again to remove harmonics from the LNA. Afterwards, it is down mixed to an IF signal that is then fed to the ADC. This architecture is widely used to receive and convert signals.

The inherent image frequency problem of the heterodyne receiver architecture gives stringent filter requirements. These requirements can be relaxed by doing double (or multi) conversion architectures[3], see Figure 2.3. In this double conversion technique several intermediate frequencies are utilized to reduce image frequencies.

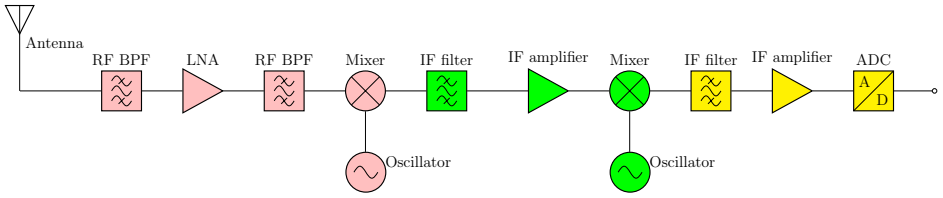

Figure 2.3: Double conversion Super-heterodyne receiver. The pink color denotes RF domain and green color denotes the 1^{st} IF domain and yellow color denotes the 2^{nd} IF domain.

The image problem can be solved by using a quadrature mixing of the signal, see Figure 2.4. The I/Q-mixing relies on accurate quadrature path matching and multi-phase clock generation to minimize I/Q imbalance, adding other constraints to the receiving architecture.

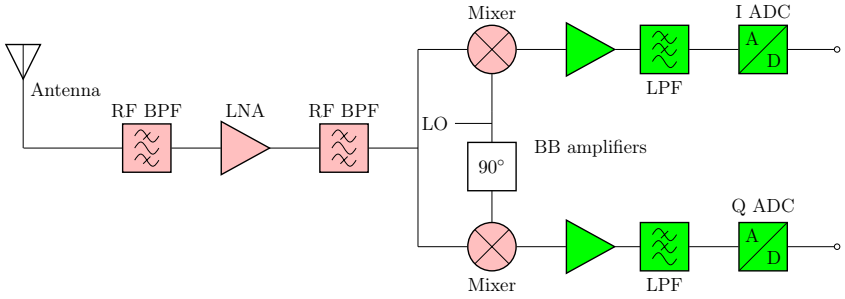

Figure 2.4: I/Q super-heterodyne receiver. The pink color denotes RF domain and green color denotes IF domain.

The short comings of the heterodyne architecture and the increased technical possibilities in circuit, architectural, and algorithmic innovations has started the search for a new receiving architecture. One proposed method for receiving architecture is direct RF sampling. This architecture utilizes a time-interleaved analog front-end, see Figure 2.5 for the block diagram representation of the receiving architecture. By focusing on increasing the sample rate, f_s, to tens of GS/s, the RF signal can be directly sampled. This removes the down mixing stage, the local oscillator is changed to a fixed clock generator and the IF filters are also removed from the receiving architecture. The sampling frequency of the architecture is

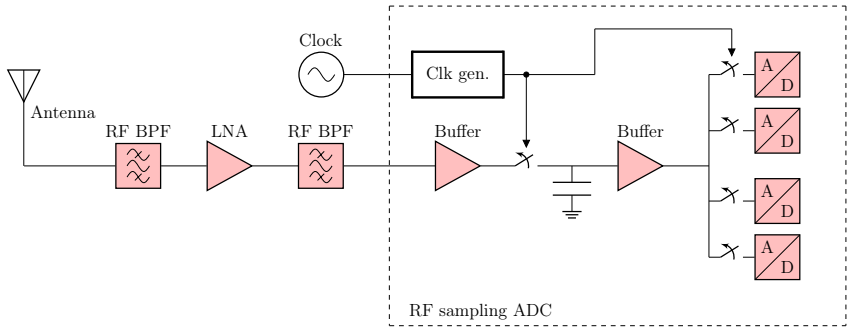

Figure 2.5: Direct RF receiver.

determined by the amount of sub-ADCs that are in parallel and their individual sampling rate.

It is this direct RF sampling method, the time-interleaved ADC architecture, that is going to be investigated in this report.

Chapter 3

Time-Interleaved Analog-to-Digital Converter Architecture

3.1 Time-Interleaved Networks

The idea of time-interleaved networks has been known for decades, it was first postulated in 1980 [4]. It is only in the last decades that the technique has been feasible to implement for tens of GHz. To increase the conversion time of the analog signal to a digital representation, D identical ADCs are time-interleaved together. Equivalently creating an ADC with a sampling rate equal to $D \cdot f_s$, where each sub-ADC has a sampling rate of f_s.

With the concept of time-interleaving the input to the sub-ADCs, the next step is to implement the analog front end to make this possible. This step requires some finesse. Many different ways are possible, but most TI ADC architectures utilize a three step approach, called a hierarchical sampling approach. The hierarchical time-interleaved network is beneficial in reducing input load and crosstalk between the different ADC channels, which improves performance over the direct sampling interleavers, [5, 6, 7].

The hierarchical approach has a parameter representation, M-N-K. Where M denotes the number of input buffers, N the number of track-and-hold (T/H) circuits with their sub-buffers, and K is the number of unit sub-ADCs. In the architecture presented, see Figure 3.1, two input buffers, $M = 2$, will share the input signal, V_{ip}, between the odd and even parts of the network. Then four 1^{st} rank track and hold circuits with a sub-buffer, $N = 4$, will divide it further to four 2^{nd} rank T/H circuits with each having a sub-ADC, $K = 4$. This results in an increased sampling rate of $32 \cdot f_{s,sub-ADC}$ as the interleaving network, $2 - 4 - 4$, gives a combined increased sample rate of $D = 2 \cdot 4 \cdot 4 = 32$. As can be seen in Figure 3.1, the front end structure of the purposed architecture is depicted. Only the positive half of the differential network is shown to make it easier to read. In the constructed network the T/H circuits are single ended. There are two parallel T/H circuits, one taking the positive input, V_{ip}, and one taking the negative input, V_{in}. The combined hold value, V_{ip} and V_{in}, is then passed to the onward for conversion. The differential path can be seen in Figure 3.2.

The hierarchical architecture with the representation of $2-4-4$ was used due to the ease of design of the clock generation network. This is becasue the base

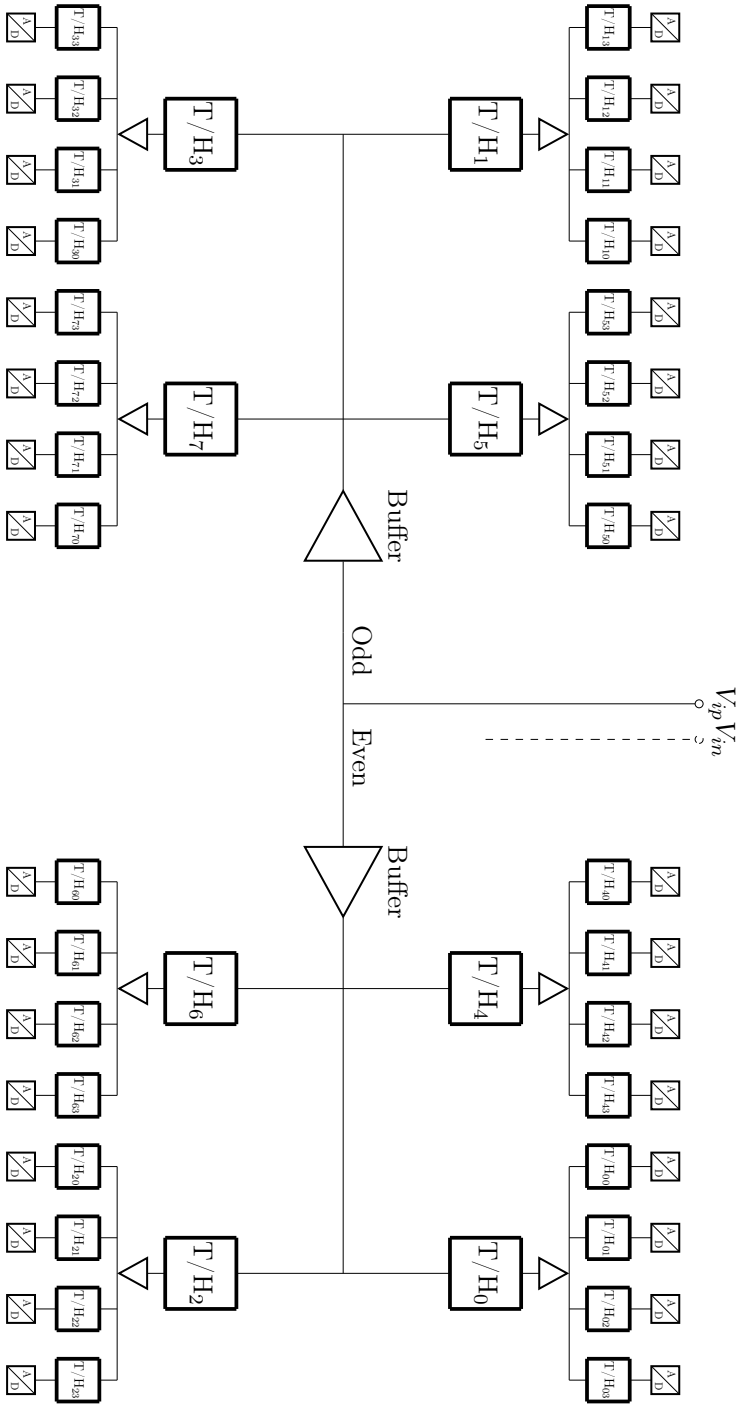

Figure 3.1: Time-interleaving analog front-end. Is a differential circuit but for simplicity only the positive half is depicted.

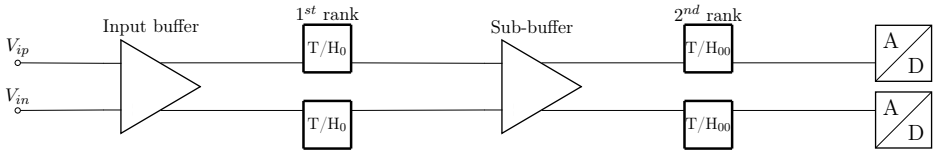

Figure 3.2: The signal path from RF to ADC.

two design can utilize dividers that divide by two. This will be further discussed in the following section 3.3.

The two different sides of the interleaved network, named Odd and Even see Figure 3.1, work 90° out of phase from each other. When the T/H_0 is in track mode, it tracks the input that comes from the input buffer. After half of the track time of T/H_0, T/H_1 starts to track the input on the Odd side of the interleaving network. This round robin schedule is repeated after all 1^{st} rank T/H circuits have tracked the input signal. See Figure 3.3 for the timing diagram of the interleaving network.

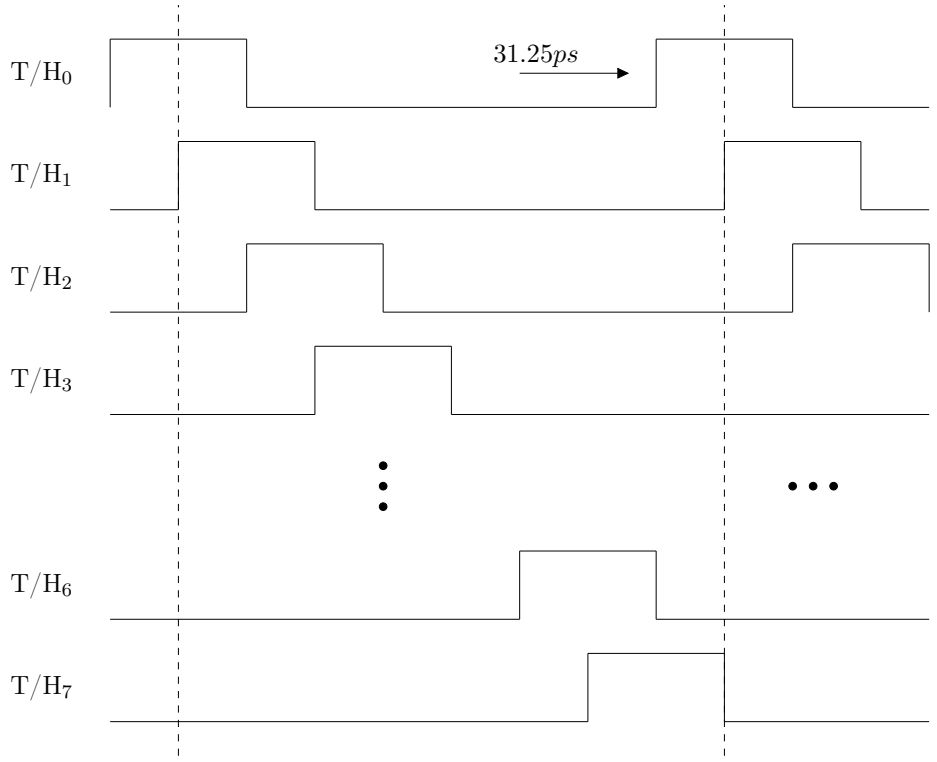

Figure 3.3: Timing diagram of the time-interleaved network. Only 1^{st} rank T/H's.

After the 1^{st} rank T/H circuits has tracked, the 2^{nd} rank T/H circuits start tracking and send the RF signal to the sub-ADC it supplies. The timing of the

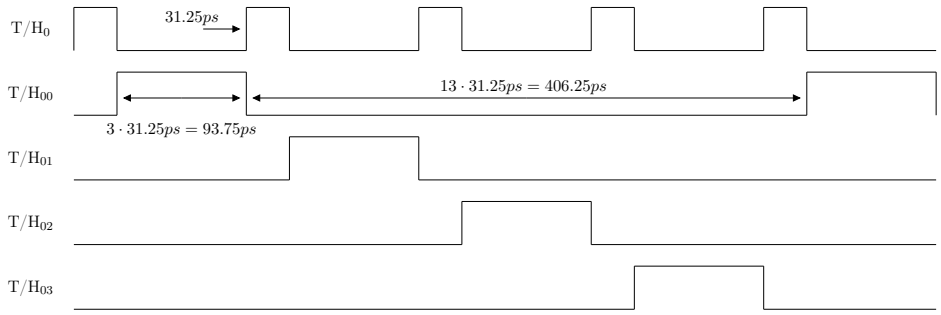

Figure 3.4: Timing between 1^{st} and 2^{nd} rank T/H.

2^{nd} rank can be seen in Figure 3.4. When the 1^{st} rank T/H is in hold mode, the 2^{nd} rank T/H starts its track mode.

The 1^{st} rank T/H circuit plays a large role in the time-interleaved network. It has to track the input and then hold the value for the following 2^{nd} rank T/H and sub-ADCs. The track time allocated to each 1^{st} rank T/H circuit is determined through this equation,

$$T_{T/H,time} = \frac{M}{f_s} = \frac{2}{64GS/s} = 31.25ps \tag{3.1}$$

In Equation 3.1, f_s is the total sample rate of the system, assuming that each sub-ADC has a sample rate of $f_{s,sub-ADC} = 2GS/s$. Having such a small track time, the construction of the T/H circuit is vital for a good functioning time-interleaved network. Because the T/H circuit is a bottleneck, [8, 9, 10], in the construction of the time-interleaved network this was the first block to be researched and constructed.

3.1.1 Track and Hold

Track and hold (T/H) circuits, often referred to as sample and hold (S/H) but in this report T/H, function is to track an voltage and then, as the name implies, hold that voltage. The decider between the phases is a switch, see Figure 3.5. During the track phase the switch is passing the input voltage onto a capacitor, C_S. When the switch is turned off, the input voltage at the moment of switching is captured on the capacitor, C_S.

This ideal switch is implemented by an NMOS switch transistor, see Figure 3.6. When the transistor is in the tracking phase, with high voltage, V_{dd}, on the gate, the input voltage is passed through the NMOS channel to the capacitor. However, the input voltage that is passed through the channel is affected by the on-resistance of the NMOS switch, see Equation 3.2.

$$R_{on} = \frac{L}{W(V_{gs} - V_{th})\mu_n C_{ox}} \tag{3.2}$$

The resistance is also affected by the input voltage as the input voltage affects the gate-source voltage, V_{gs}, see Equation 3.4[11].

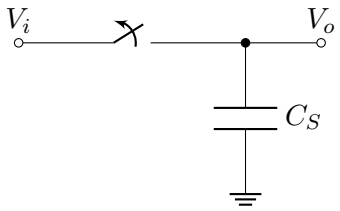

Figure 3.5: Ideal track and hold circuit.

$$V_{gs} = V_{dd} - V_i \tag{3.3}$$

$$R_{on} = \frac{L}{W(V_{dd} - V_{in} - V_{th})\mu_n C_{ox}} \tag{3.4}$$

From the equations it can be seen that R_{on} is dependent on the gate voltage and also the input voltage. This leads to two conclusions, that a high gate voltage will lower the on-resistance and that the input has an effect on the channel resistance. As the input voltage increases or decreases during the track phase a non-linear effect is created. To mitigate these non-idealities a bootstrap circuit is implemented. The bootstrap circuit applies a higher voltage, $> V_{dd}$, on the gate and also passes the input voltage variation onto the gate. This has the effect of reducing the R_{on} and also removing the non-linear dependence of the input voltage. The equation for the on-resistance becomes,

$$V_{gs} = V_{gate} - V_{source} = V_{bst} - V_{in} \tag{3.5}$$

$$V_{bst} = V_{dd} + V_{in} \tag{3.6}$$

$$R_{on} = \frac{L}{W(V_{bst} - V_{in} - V_{th})\mu_n C_{ox}} = \frac{L}{W(V_{dd} - V_{th})\mu_n C_{ox}} \tag{3.7}$$

The voltage V_{bst} is the voltage created from the bootstrap circuit for the gate of the switch transistor. In Equation 3.7, the non-linear effect from the input voltage has been removed. Effectively creating a linear low resistance pass-transistor. The construction of a bootstrap circuit can be done in several ways. In the following sections, one method will be described and with it some improvement techniques.

Conventional Bootstrap Circuit

The conventional bootstrap circuit, see Figure 3.7, applies an increased voltage on the switch's gate, simultaneously reducing the R_{on} and the dependency of the input voltage, V_{in}. The bootstrapped T/H circuit is working in two different modes. In the hold mode the signal Clk_b is high and then Clk is correspondingly low. The goal with the hold mode is to charge V_{dd} over the capacitor, C_B. This charging is done through the transistors M_2 and M_3. They are controlled with the Clk_b signal that opens M_7 and then passes ground to the gate of M_2 through M_6 and M_7, it passes ground to the gates of M_{switch} and M_1 also. The transistor

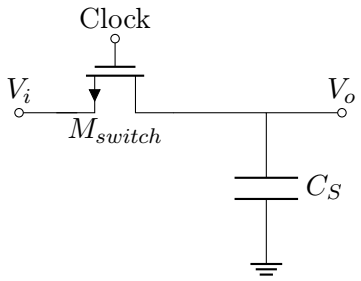

Figure 3.6: Track and hold circuit with NMOS switch.

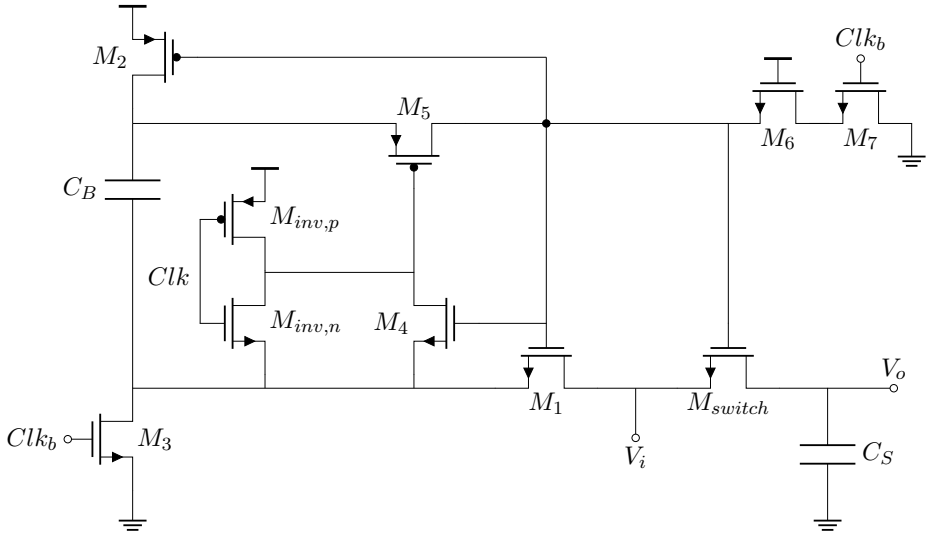

Figure 3.7: Conventional bootstrap T/H.

M_5 is kept closed with the inverter circuit, $M_{inv,p}$ and $M_{inv,p}$, setting its gate to high.

Then, when the track mode is initiated, Clk_b is set to low. This turns off M_3 which closes the path to the ground for the bottom of the capacitor, C_B, and to the gates of M_1, M_2, M_4, and M_{switch}. The inverter circuit pulls the low voltage of the bottom plate of the capacitor to the gate of M_5. This makes so the high voltage over the capacitor is shared over the gates of the transistors M_1, M_2, M_4, and M_{switch}. This in turn, turns on M_1, M_4, and M_{switch}, and turns off M_2. The turned on M_1 passes the input voltage to the bottom plate of the capacitor. The capacitor wants to keep the same voltage over its plates so the voltage on the top plate is increased, giving a high voltage to the gate of M_{switch} making the on-resistance low. As the input voltage is passed to the bottom plate, the gate voltages of M_1, M_4, and M_{switch} inherit the input voltage variation, removing the non-linear effect.

The capacitor is utilized as a battery to load the boosted voltage on the node

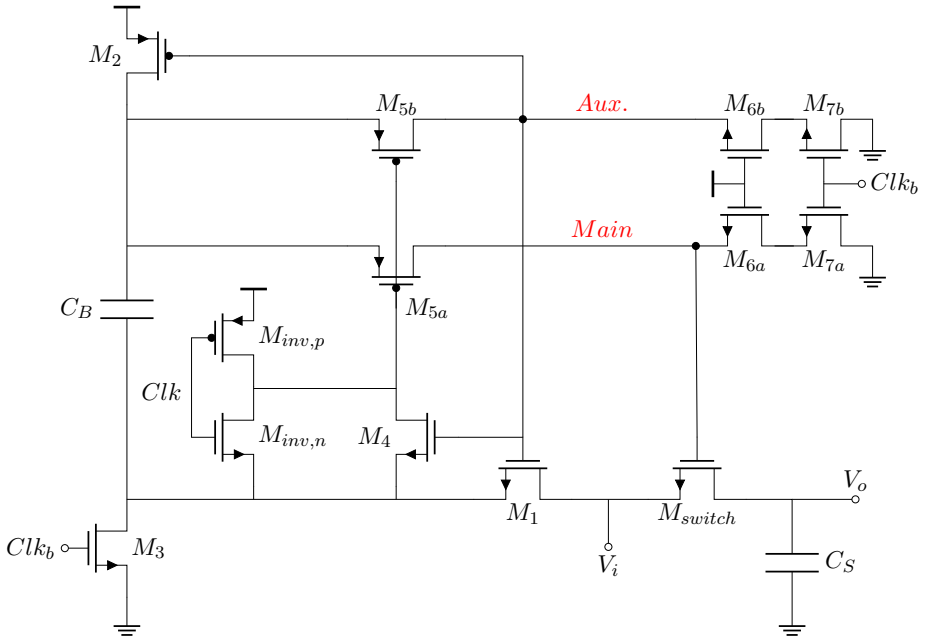

Figure 3.8: Auxiliary path bootstrap T/H.

to which the M_{switch} gate is connected. A voltage division is made when the bootstrap circuit gets into track mode. The voltage division will between all the parasitic capacitance in that node, the gates of M_1, M_2, M_4, and M_{switch}, and the capacitor C_B. To increase the effectiveness of the bootstrap circuit, two improvements can be made. Introducing an auxiliary path, see Figure 3.8, reduces the parasitic capacitance at the critical node when the node is discharged. Another improvement technique is dual path or fully split bootstrap, see Figure 3.9. This improvement builds on the auxiliary path circuit but also splits the capacitor, C_B, into two parallel capacitors. This way, the voltage division is lowered and the rise- and fall-time of the gate voltage of M_{switch} is lowered also.

Auxiliary Path Bootstrap

In Figure 3.8 the auxiliary path bootstrap circuit can be seen. The difference between the conventional bootstrap circuit and auxiliary path bootstrap circuit is the addition of another path. The transistors M_5, M_6, and M_7 are duplicated and used to create a new identical path. These two identical paths are called main and auxiliary, Main and Aux in the Figure 3.8. By doing this, the discharge, when going from track mode to hold mode, of the boosted voltage on the gate of M_{switch} can be done quicker, as the gate is discharged by a separate circuit than the auxiliary path. The transistors M_{6a} and M_{7a} discharge the main path quicker than the auxiliary path as the parasitic capacitance is lower, the number of gates on the main path is 1 and the auxiliary path is 2.

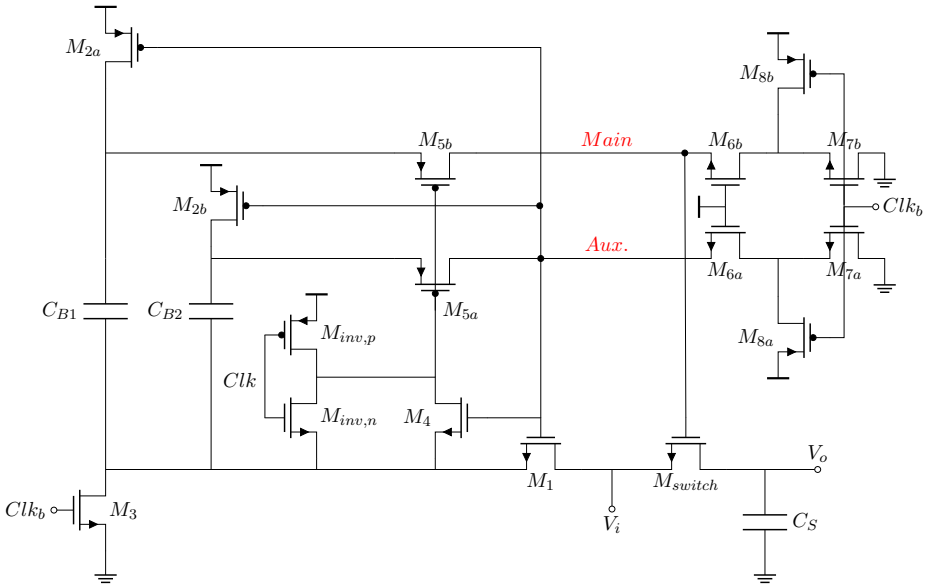

Figure 3.9: Fully split bootstrap T/H.

Fully Split Bootstrap

In Figure 3.9 the fully split bootstrap circuit can be seen. The difference from the auxiliary path is that the capacitor has been split into two capacitors, C_{B1} and C_{B2}. This makes the gate of M_{switch} only connected to the necessary charging and discharging part of the bootstrap circuit. The voltage division is reduced as the gate of M_{switch} is the only gate that is loading the capacitor C_{B1}. This speeds up the rise-time. To increase rise-time the transistors M_{8a} and M_{8b} have also been added. When Clk_b becomes high, M_{8a} and M_{8b} pull V_{dd} down to the Main and auxiliary path. This changes the voltage division between the parasitic capacitance and the capacitors C_{B1} and C_{B2}, since the voltage at the gates of M_1, M_{2a}, M_{2b}, M_4, and M_{switch} is at a higher potential before M_{5a} and M_{5b} are open and conducting.

Nonidealities with the T/H

The construction of the bootstrap circuit is done and the function of the circuit is satisfying, however some added benefits can be done to mitigate circuit nonidealities. Three different non-idealizes exist in the bootstrap circuit: signal feedthrough, charge injection, and clock feedthrough [7].

The signal feedthrough can be observed in Figure 3.10. The input signal is fed through the M_{switch}, see Figure 3.9. This, having a high effect on output voltage, can vary the captured and decoded value that the ADC captures. This will create an error. To minimize this, a signal feedthrough compensation technique can be used, this can be done with an always off dummy bootstrap network, with no capacitors to reduce area. In this dummy network the negative input is used. This

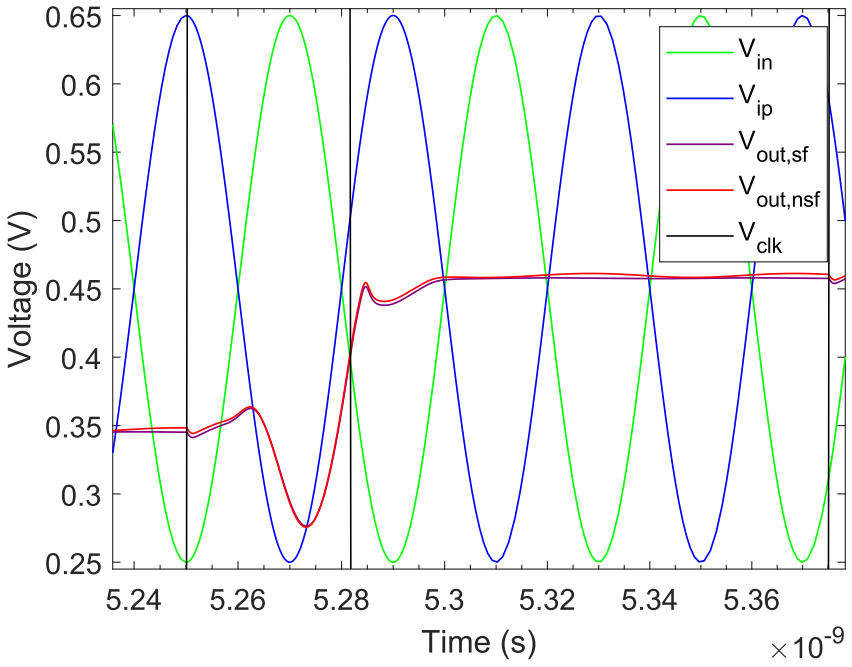

Figure 3.10: Two implementation of the T/H circuit, one with signal feedthrough compensation($V_{out,sf}$) and one without($V_{out,nsf}$).

method reduces the ripple that can be seen on the hold capacitor, C_S, minimizing errors. The dummy bootstrap circuit is the same as the fully split bootstrap[5], [12].

Charge injection occurs when the main switch goes from "ON" to "OFF", the channel collapses and the residual charge in the channel is injected into the circuit, through the drain and source. In the T/H case, this injection of charge lowers or increases the hold voltage over the capacitance, creating a hold error. The amount of charge in the channel at the moment of switching between the "ON" and "OFF" states depends on the input voltage. Techniques have been investigated to mitigate this error. One technique is to utilize one or several dummy transistors. These dummy transistors are fed with an inverted gate signal to the main switch and its source and drain are coupled together. When the main switch is switched to the "OFF" state, the charge still in the channel is absorbed by the dummy transistor that is switched "ON". This technique reduces the charge injection, leading to a reduction in holding error [13].

Clock feedthrough is a capacitance effect that occurs from the parasitic C_{gs} and C_{gd}. When the gate is clocked from high to low, the parasitic capacitance wants to keep the voltage difference. This would push the voltage at the output through capacitive coupling. Clock feedthrough is an intrinsic non-ideality and compensation for it has not been implemented. To keep effects low from clock

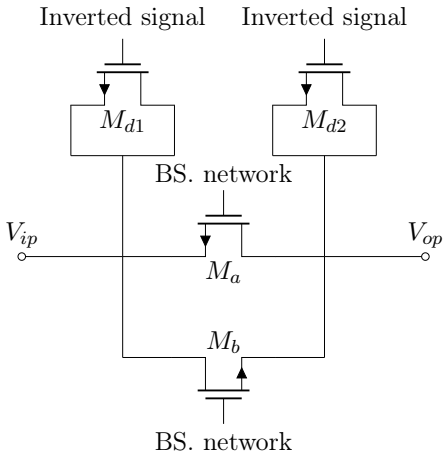

Figure 3.11: T/H switch with dummy transistors.

feedthrough, the size of the switch is to be kept low [14].

The constructed switch used can be seen in Figure 3.11. The switch has been split into two parts, where the drain and source are connected to reduce the process effects when the transistors is made, gate-drain and gate-source can be different sizes so this technique creates an equal charge injection for both ports of the switch. The newly split transistors, M_a and M_b, widths are half of M_{switch}, see Figure 3.9. The other transistors, M_{d1} and M_{d2}, are the dummy transistors that will absorb the charge from the channel when the main switch, M_a and M_b, is turned off. Their width is half of M_{switch}.

Complete T/H Circuit

The complete T/H circuit used in this report can be seen in Figure 3.12. Here the new switch can be seen with its dummy transistors to minimize the charge injection effect. The dummy BS. is represented by a box, and it is used to minimize the signal feedthrough. Another change is that the drains of M_{7a} and M_{7b} have been connected to a $150mV$ voltage source. This added change has made the rise-time faster for the track mode. As the main and auxiliary path already is loaded with a voltage, the charging from the capacitors C_{B1} and C_{B1} is faster.

3.1.2 Input Buffer

The purpose of the input buffer is to isolate the two different paths, Odd and Even from each other, see Figure 3.1. As they are being clocked separately and have T/Hs that track at the same time, the loading of the input would change irregularly if they were connected. To mitigate this effect, the buffers keep the input load constant and separate the two different branches.

The buffer is a PMOS source follower, see Figure 3.13. The PMOS buffer is chosen because the input has no dc part, which means that the input varies around

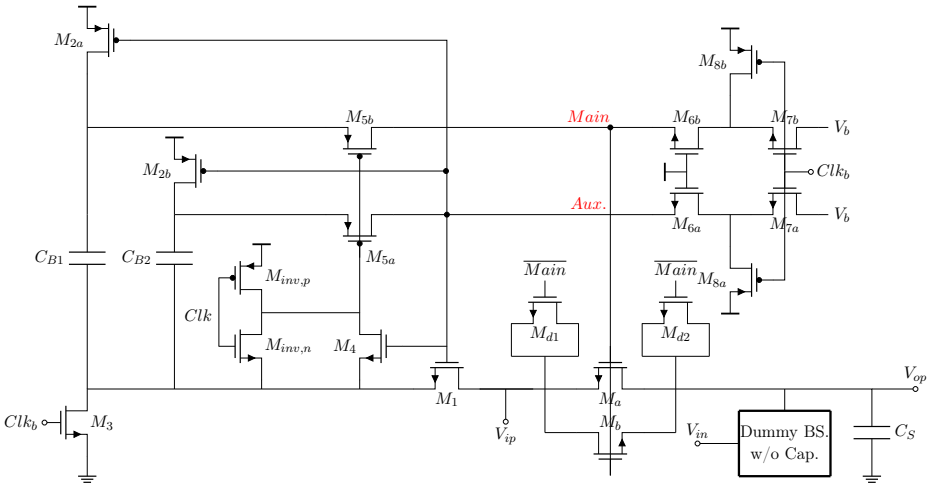

Figure 3.12: Complete T/H circuit, with signal feedthrough and charge injection compensation.

ground, $V = 0V$. The bias voltage, V_b, is chosen so that the output dc voltage level is at $V_{o,dc} = 450mV$. The rail voltage is changed for this block to a value of $V_{dd} = 1.1V$, this is to increase the gain and bandwidth of the stage. As the input of the buffer will be an RF signal, the bandwidth needs to be very wide, approximately $32GHz$, to avoid distortion of the input signal.

3.1.3 Sub-buffer

The construction of the sub-buffer is done with an NMOS source follower, see Figure 3.14. An NMOS design was chosen because the input voltage of the sub-buffer has a DC part of $450mV$. The objective of the sub-buffer is to buffer the input from the 1^{st} rank T/H. Having a buffer reduces the capacitance seen of the 1^{st} rank T/H, easing the design of the T/H. The design of the sub-buffer had to take into account the input capacitance of the ADC during the construction. The intended sub-ADC for the time-interleaving network has an input capacitance of $1pF$. Therefore, this load capacitance was used. The bandwidth of the sub-buffer is $BW \approx 10GHz$. This low bandwidth is due to the fact that the input to the sub-buffer is a static voltage with an AC part during the 1^{st} rank T/H track phase.

3.1.4 2^{nd} Rank T/H

The roll of the 2^{nd} rank T/H is to hold the voltage for the sub-buffers. The T/H's design is an auxiliary path bootstrap circuit, see Figure 3.15. The track and hold time can be seen in Figure 3.4. A charge injection compensation switch is implemented. A signal feedthrough compensation circuit is not implemented because the input signal to the T/H has such a low ac voltage part making the compensation circuit redundant.

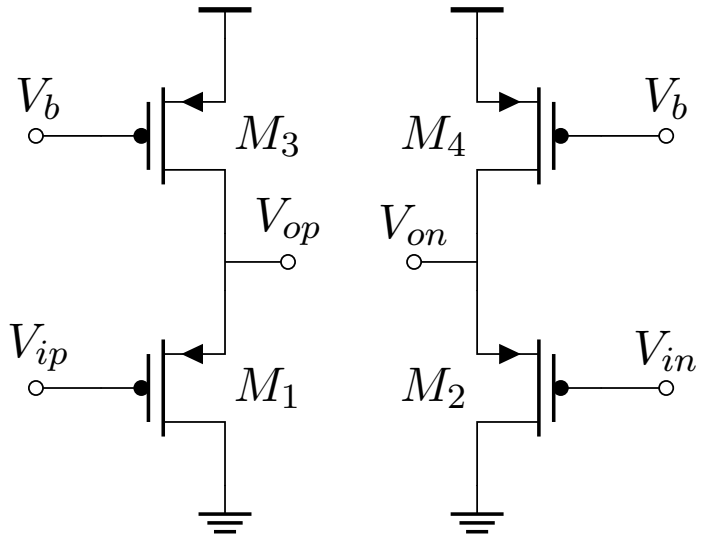

Figure 3.13: Input buffer.

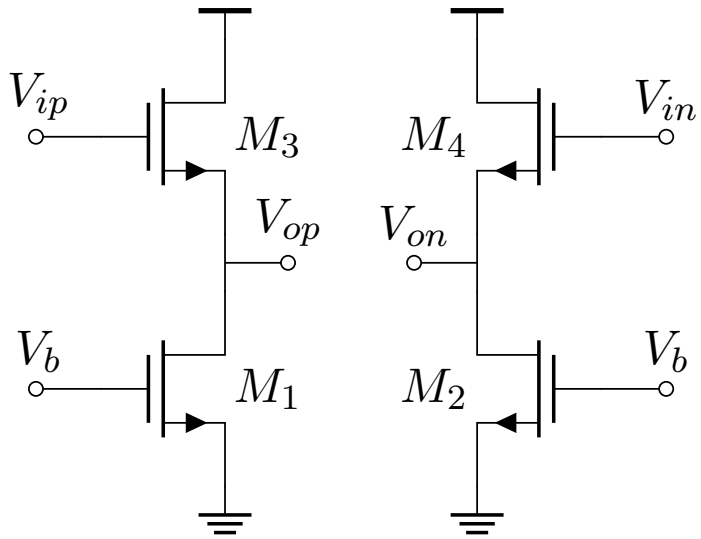

Figure 3.14: Sub-buffer.

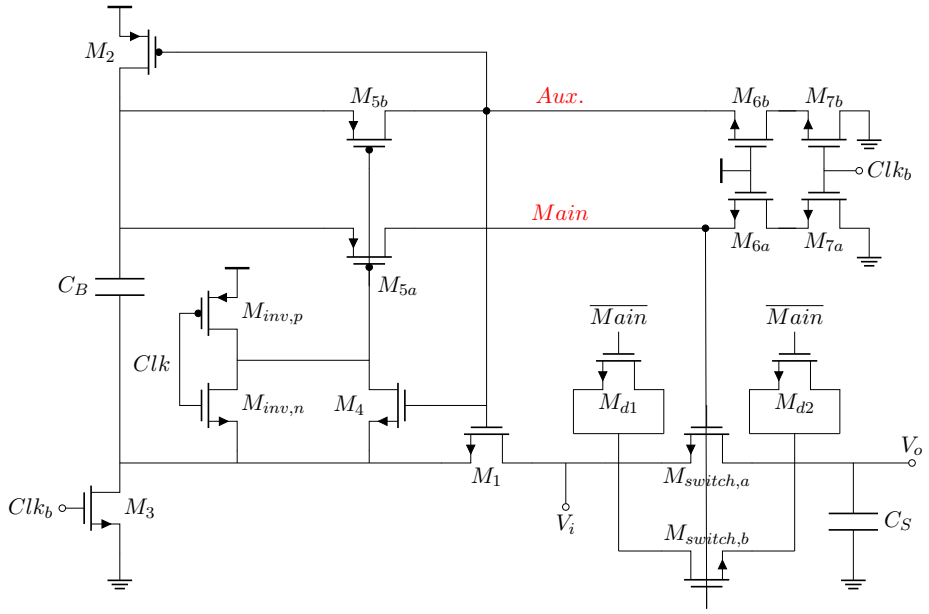

Figure 3.15: 2^{nd} rank T/H.

3.2 Mismatch of TI Networks

The complete system is being built on multiple similar smaller blocks, which during production can undergo different process variations, PVT variations, creating mismatches in the TI network. When the digital output from the sub-ADCs are time-demultiplexed into a single data stream, the mixing of inevitable mismatches among sub-ADCs and other blocks in the time-interleaved network introduces non-negligible spurious spectral content. These mismatches in time-interleaved networks can be categorized: 1) offset; 2) gain error; 3) bandwidth among the time-interleaved samplers and quantizers; and 4) sampling time skew [6].

The offset mismatch depends on the varied offsets that the signal chain imposes on the input signal. This means that for a DC input, each ADC would produce a different output code. This will appear with a period of D/f_s in the output converted signal, where D is the number of sub-ADCs. In the frequency domain, this would introduce spurs at the frequencies [15],

$$f_{offset} = k \cdot f_s/D, \qquad k = 0, 1, 2, ... \tag{3.8}$$

Gain mismatches are introduced from different gains in the buffers. The error will be, as with the offset, with a period of D/f_s. However, the magnitude is modulated by the input frequency. Leading to an amplitude modulation like error distribution. The frequency spurs will be located at,

$$f_{gain} = \pm f_{in} + \frac{k}{D} f_s, \qquad k = 1, 2, 3, ... \tag{3.9}$$

Bandwidth mismatch between the channels is a non-ideality that is described with a first-order system approximation. The different channels can be described by an RC system. Especially the T/H circuits, having an on-resistance depending on PVT variations and holding capacitors. The frequency transfer function becomes,

$$H(\omega) = \frac{1}{1 + j\omega RC} \tag{3.10}$$

Here, R and C are the first-order resistance and capacitance representations of the system. As variations will be present after fabrication, the different channels will manipulate the input differently as the resistance and capacitance will vary. This leads to a bandwidth mismatch resulting in frequency spurs at,

$$f_{bw} = \pm f_{in} + \frac{k}{M \cdot N} f_s, \qquad k = 1, 2, 3, ... \tag{3.11}$$

Where M and N are the number of input buffers and 1^{st} rank T/H circuits, respectively.

The last mismatch causing spurious input images is sampling time skew. There are two kinds of timing errors in a TI network, clock skew (systematic error) and clock jitter (random error) [15]. Jitter is unavoidable but can be manged, clock skew is the main suspect. If the clocking of the T/H is skewed from the ideal timing the captured value is erroneous. The largest variation in the captured value occurs when the input signal has the largest slew rate. This mismatch gives rise to spurs in the frequency domain, the spurs follow the same periodicity as gain mismatch,

$$f_{skew} = \pm f_{in} + \frac{k}{D} f_s, \qquad k = 1, 2, 3, ... \tag{3.12}$$

Due to these mismatches, the output spectrum from the ADC will show additional images of the input signal at different frequencies and power levels. These spurs in the frequency spectrum are known as interleaving spurious signals or TI spurs or artifacts. To mitigate these introduced TI spurs, calibration is needed for the time-interleaved networks. Different calibration options exist and are described in brief in the Appendix, but are out of the scope of the report.

Up until now, ideal clocking has been assumed for the circuit. However, no ideal clock exists so the next step in the thesis is to create a clocking network for the TI ADC.

3.3 Clock Generation

The timing of the interleaving network is vital for a working TI ADC network. To capture a true representation of the RF signal, the captured samples have to be well defined. To have a well defined clock with low jitter and low skew, one needs to start with a common clock source. The clock generation starts with a differential $32GHz$ sinusoidal signal, assumed to be created by a on-chip phase locked-loop (PLL). These signals are then divided into the required frequencies and duty cycles. As can be seen in Figure 3.16

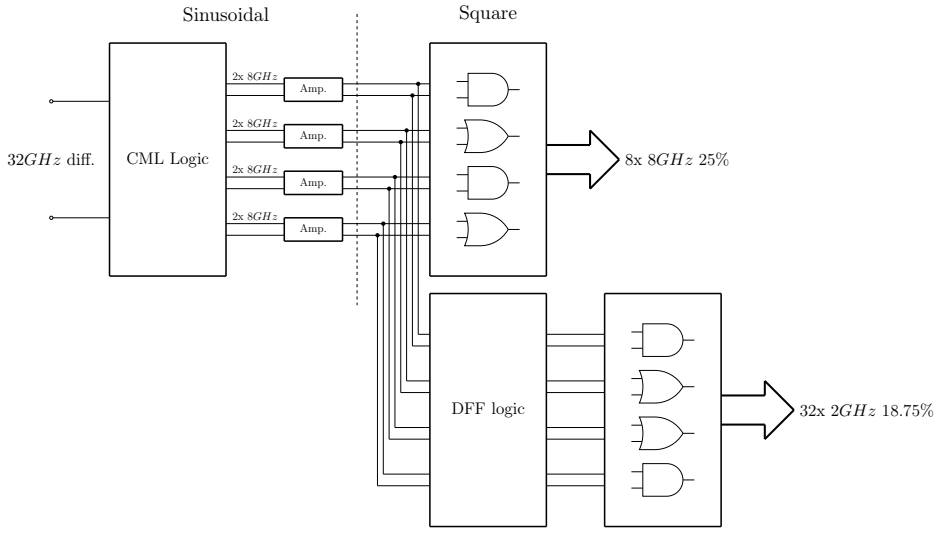

Figure 3.16: Clock generation of 1^{st} rank T/H.

3.3.1 Current Mode Logic

To create the signals for the 1^{st} rank T/H's, the high frequency $32GHz$ sinusoidal signal is down converted using four current mode logic (CML) latches in series, see Figure 3.17, [16]. The configuration seen in Figure 3.18 effectively divides the differential $32GHz$ signal into eight $8GHz$ signals, [17], [18]. As can be seen in Figure 3.19 the CML is biased through a high-pass filter, where the $32GHz$ signal is the input.

An earlier iteration of clock generation utilized a differential DFF, [19]. The CML then only divided the $32GHz$ signal into four $16GHz$ signals. The further division to $8GHz$ signals used a DFF, and this implementation reduced the current consumption. However, the DFF blocks are prone to be easily effected by loads. This resulted in a decision of using a higher order division with the CML latch blocks instead.

3.3.2 Sinusoidal to Square Wave Conversion

After the CML divider the signal has to be converted to square waves. This is done via an amplifier stage, see Figure 3.20. The capacitor is a DC block to not disturb biasing and is also a tuning parameter to create resonance at $8GHz$. The amplification of the stage effectively sets high voltages to V_{dd} and low voltages to ground, creating a square wave. The results are eight $8GHz$ square wave signals that are 45° off phase to each other.

3.3.3 Gate Logic

The generation of the specific duty cycles for the 1^{st} rank T/H is done with logic gates. As can be seen in Figure 3.21, using the AND logic gate and combining

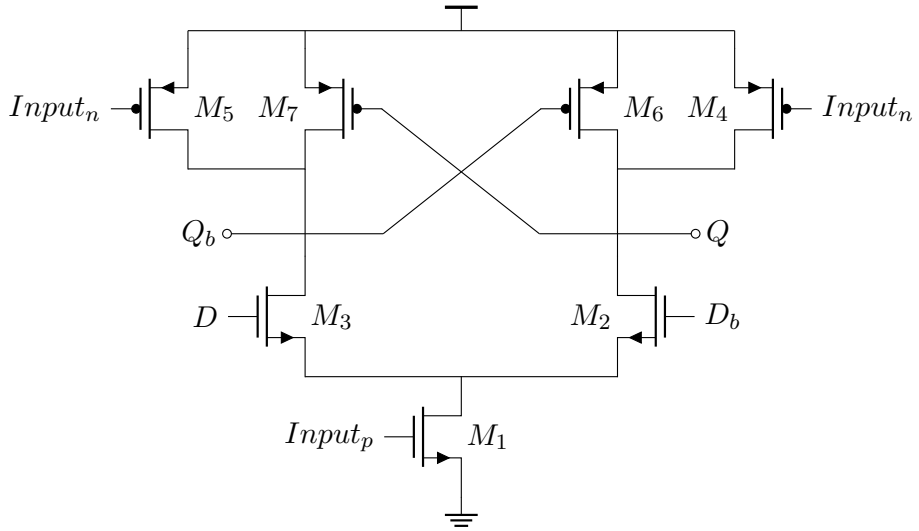

Figure 3.17: Current mode logic.

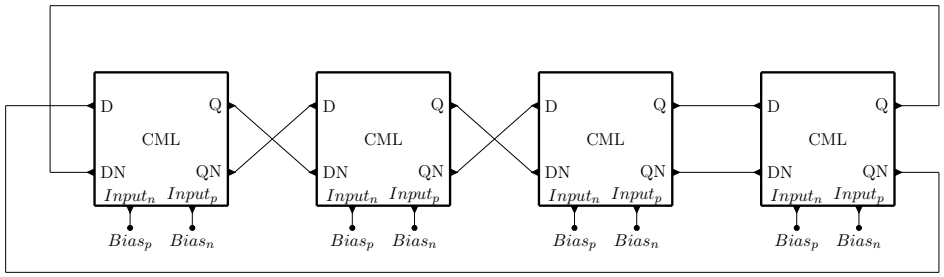

Figure 3.18: CML divider.

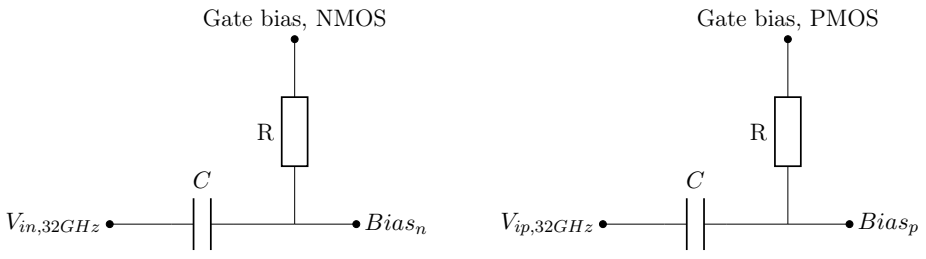

Figure 3.19: Bias network for CML divider.

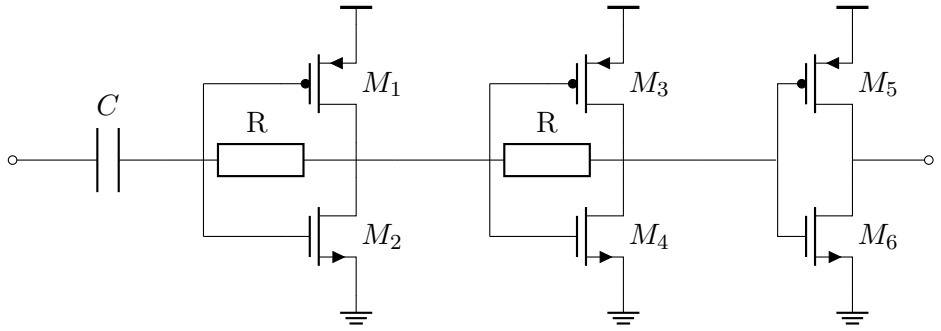

Figure 3.20: Amplification stage.

the $8GHz$ signals that are 90° off phase to each other generates a duty cycle of 25%. This is done for all the possible combination, generating the signals for the 1^{st} rank T/H. The inverted signal of the clocks, CLK_b, are generated by using a NOR gate instead.

3.3.4 Second Rank T/H

For the generation of the 32 $2GHz$ 18.75% clock signals, a divide-by-4 block is used. It is implemented with a differential digital flip-flop (DFF), see Figure 3.22. Connecting two Dff block in series as seen in Figure 3.23, each $8GHz$ signal creates four $2GHz$ signals. This results in 32 $2GHz$ signals with a duty cycle of 50%. With the same technique for the generation of 25% duty cycle for $8GHz$ AND gate logic is used for the $2GHz$.

The specific duty cycle of 18.75% is than created with an AND gate with the input signals of clk_b for the 1^{st} rank T/H and the $2GHz$ 25% duty cycle signals.

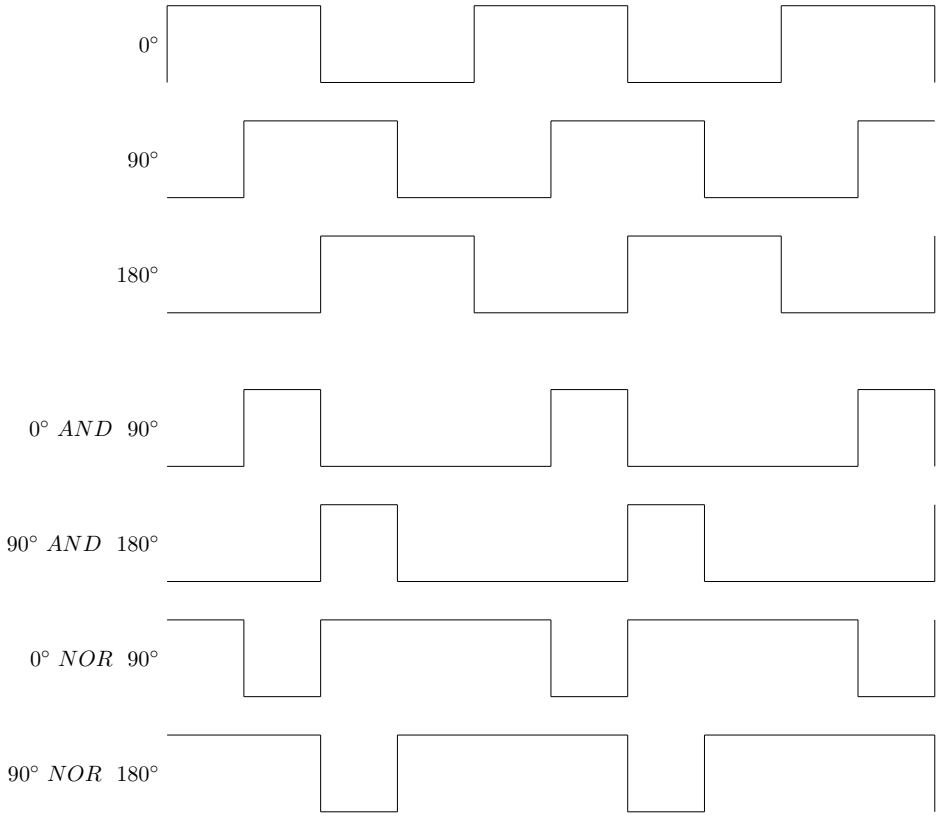

Figure 3.21: Generation of 1^{st} rank T/H clock signals.

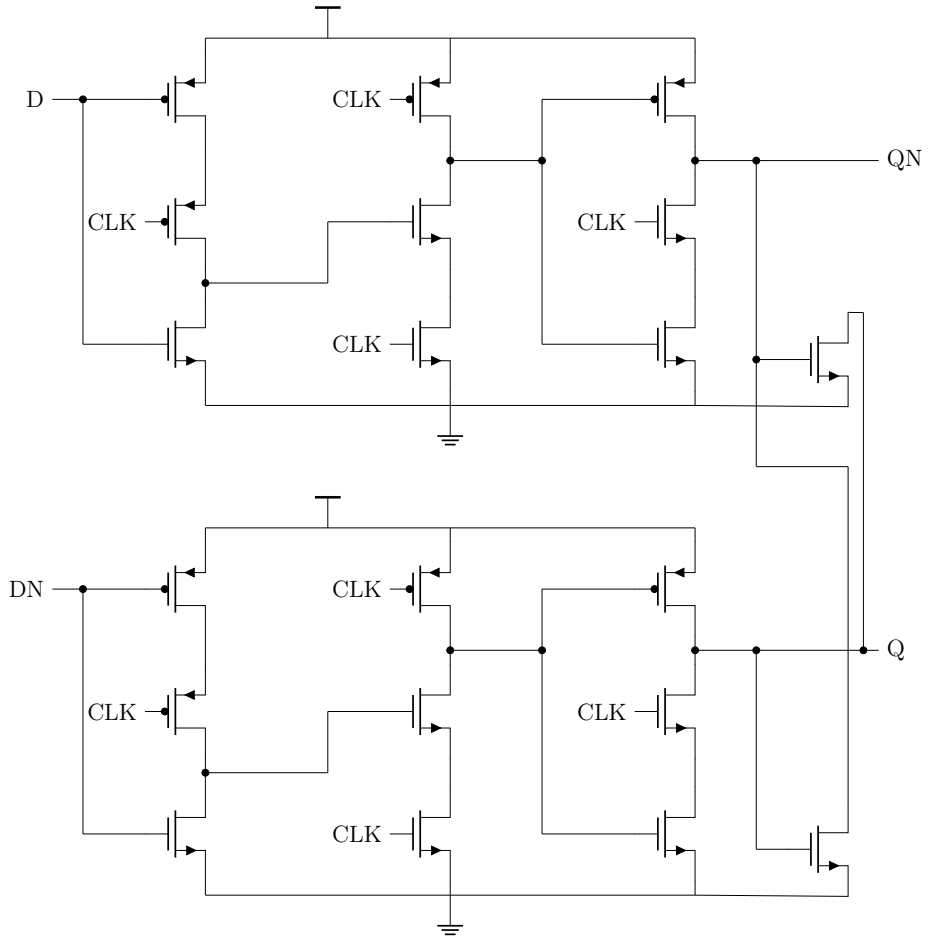

Figure 3.22: Differential digital flip-flop constructed with two TSPC's.

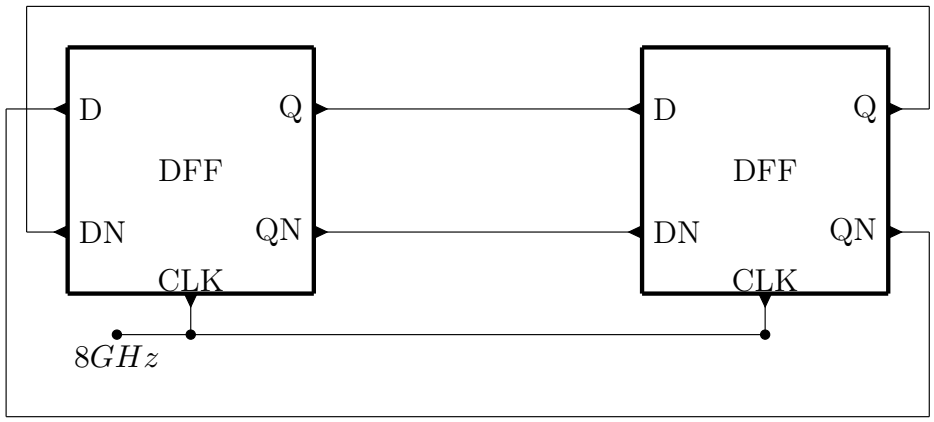

Figure 3.23: DFF divide-by-4.

Chapter 4
Results

4.1 Complete System

The two systems, the clock generation and the time-interleaving network, were combined. The functionality and limits of the time-interleaved network and clock generation were simulated both separately and in combination.

The complete system have many sources of non-idealities. These come from both the TI network and the clock generation. Therefore, to understand all the non-idealities, the blocks need to undergo different types of tests before the full system can be evaluated.

4.1.1 Complete System with Ideal Clock Generation

The TI network is connected to an ideal clock generation circuit. This will make it possible to investigate the non-idealities that only the TI network contributes with.

Since the TI network is in principle a larger sampling circuit, the verification becomes that the output maps to the input. Meaning that the frequency of the sampled output holds the same value as the input signal.

FFT

During this part of the report the results from the ideal clocked TI network is presented.

From Figure 4.1 we notice that SFDR increases with frequency up until a point where it starts to decrease. This is not realistic behavior, even though there is no added noise or other distortion to the circuit. Considering the circuit investigated being a time-interleaving network, with T/Hs and buffers, the most reasonable contributor is assumed to be the charge-injection compensation switch. Due to the peak in SFDR at $15GHz$, it points to an optimum sizing of the switch for that frequency. This because the designing process of the T/H was done with an input frequency of $15GHz$. For lower and higher input frequencies, the compensation may not match as well to the input signal's voltage level during the falling edge of the tracking clock. This effect was not known about during the design process of the T/H. If it had been known, the input frequency during design would be varied.

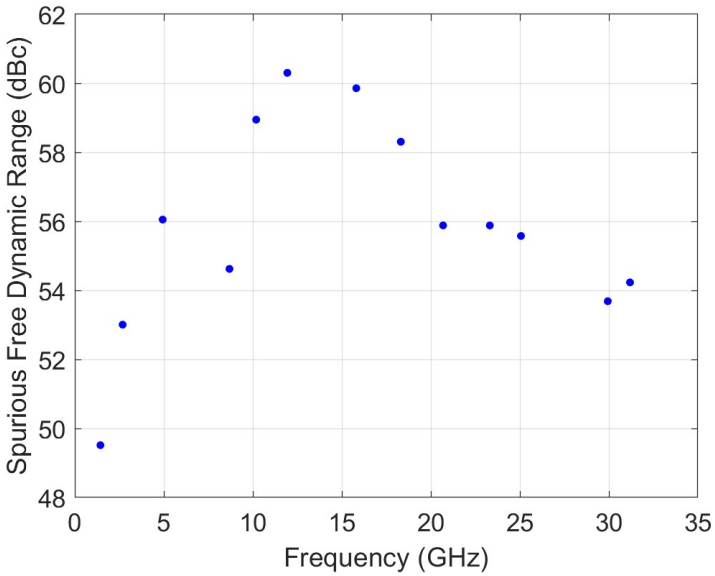

Figure 4.1: SFDR of the ideal clocked TI network.

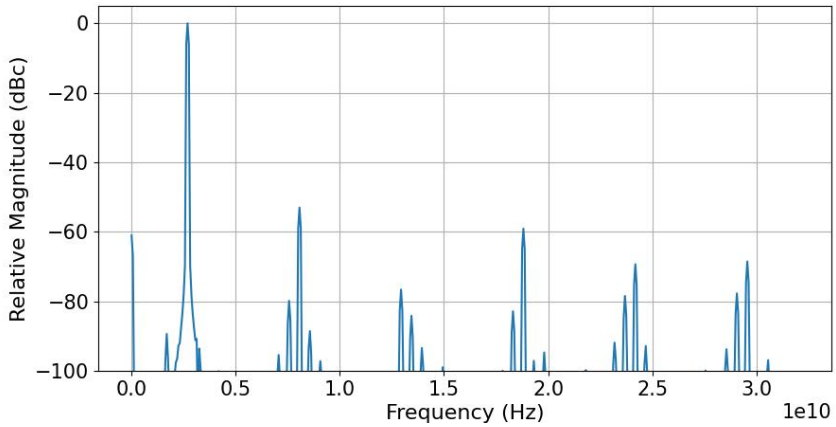

Figure 4.2: FFT of sampled output with input frequency at $f_{in} = 2.6875GHz$. Ideal clocking.

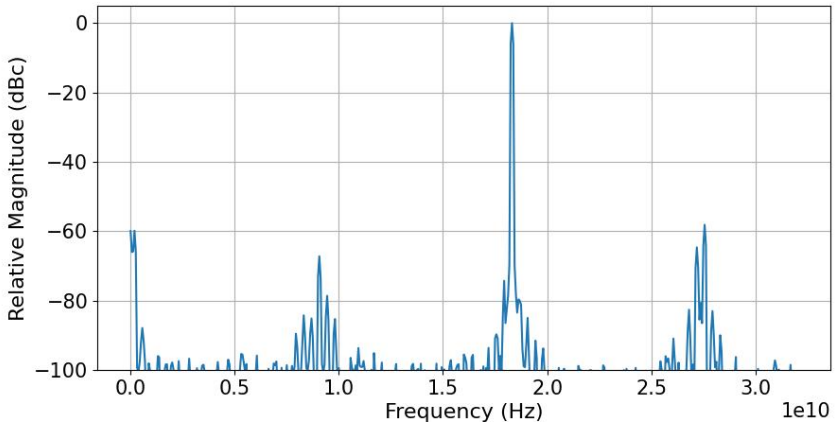

Figure 4.3: FFT of sampled output with input frequency at $f_{in} = 18.3125GHz$. Ideal clocking.

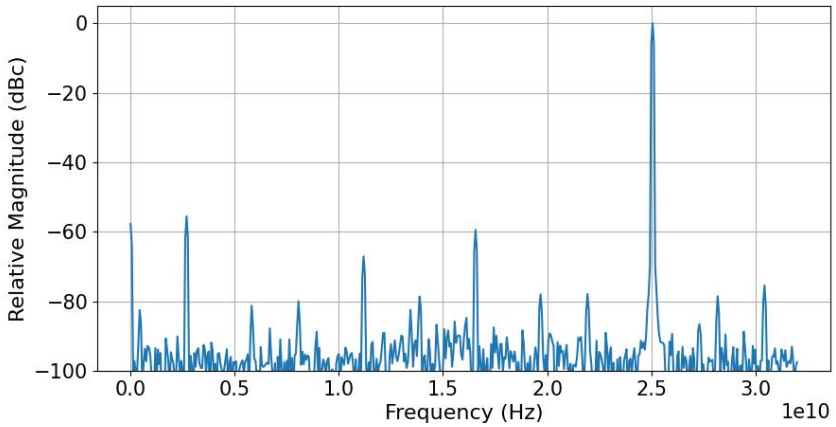

Figure 4.4: FFT of sampled output with input frequency at $f_{in} = 25.0625GHz$. Ideal clocking.

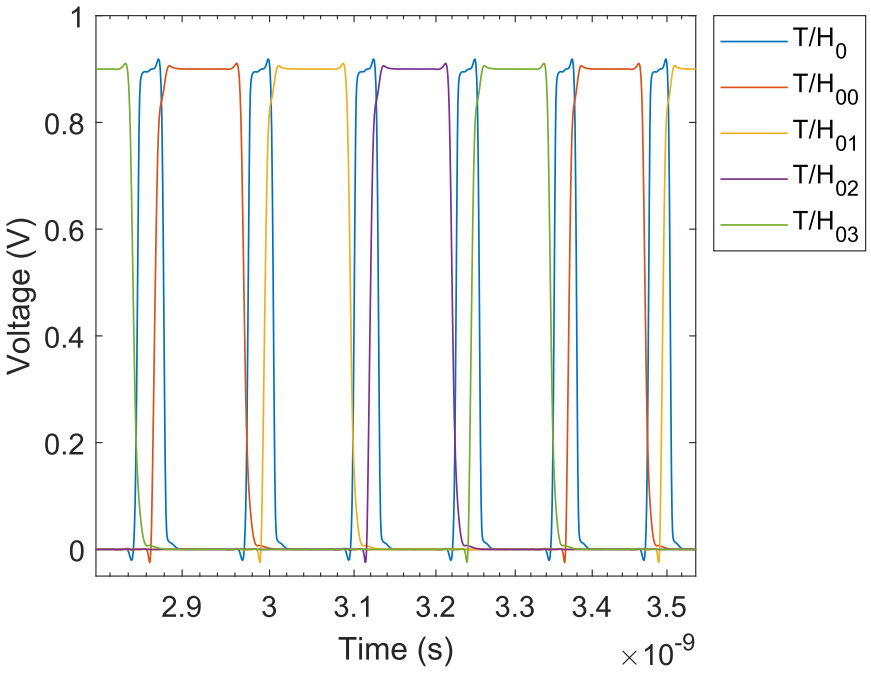

Figure 4.5: The clocks for 1^{st} and 2^{nd} rank T/H's generated by the network.

4.1.2 Clock Generation Network

In this section, the function of the clock generation network will be investigated. In Figure 4.5 the generated clocks for one of the leaves can be observed. There is an overlap between the 1^{st} rank clock and the 2^{nd} rank clock, this has to do with the fact that the 2^{nd} rank clock are generated by the 1^{st} rank clock. However, since the overlap occurs at the negative edge of the 1^{st} rank clock and not the positive, the tracked value that the 2^{nd} rank T/H has will not be affected.

Frequency Dividers

For a functional system, the frequency dividers need to produce a stable output frequency. The presented topology consists of a CML divide-by-4 and a DFF divide-by-4 dividers. The CML divider divides the input $32GHz$ frequency to $8GHz$ and these $8GHz$ clocks are then divided using DFF to $2GHz$. In Figures 4.6 and 4.7 stable frequencies for both the CML and DFF dividers can be seen. There is some variation in frequency, however, not enough to diminish the sampling.

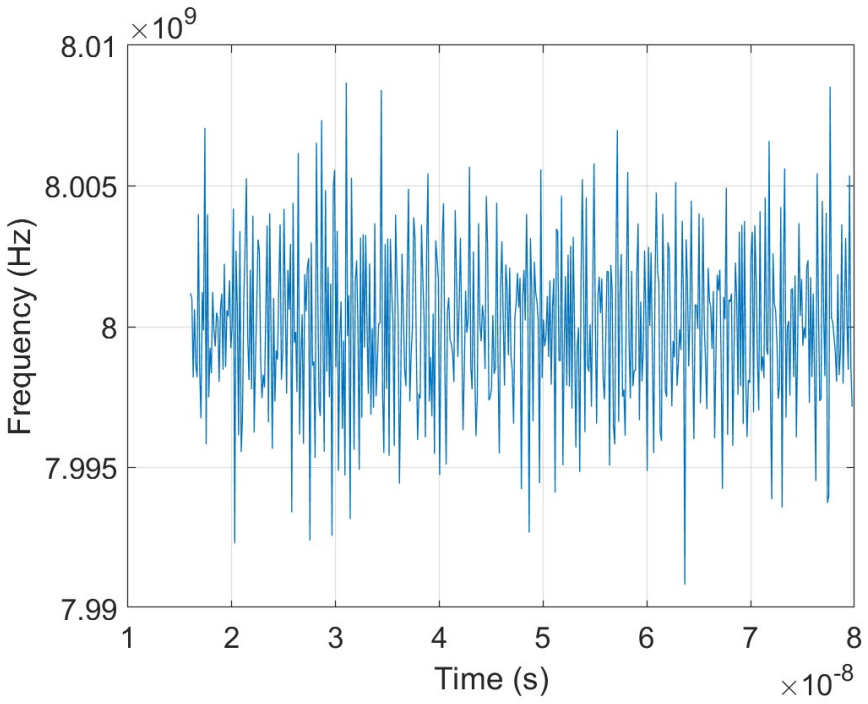

Figure 4.6: Frequency stability for the CML clock divider.

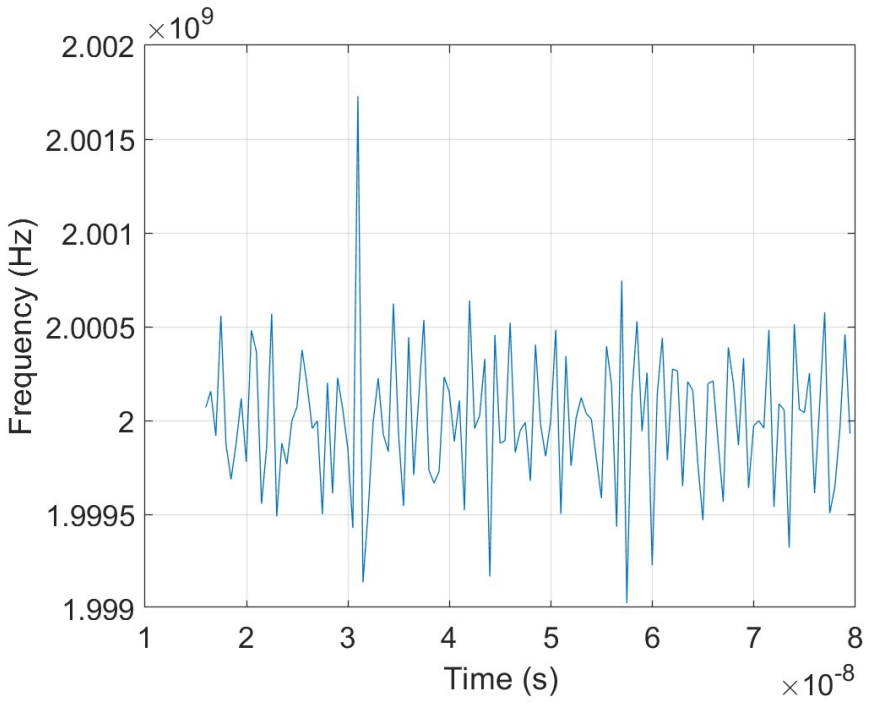

Figure 4.7: Frequency stability for the DFF clock divider.

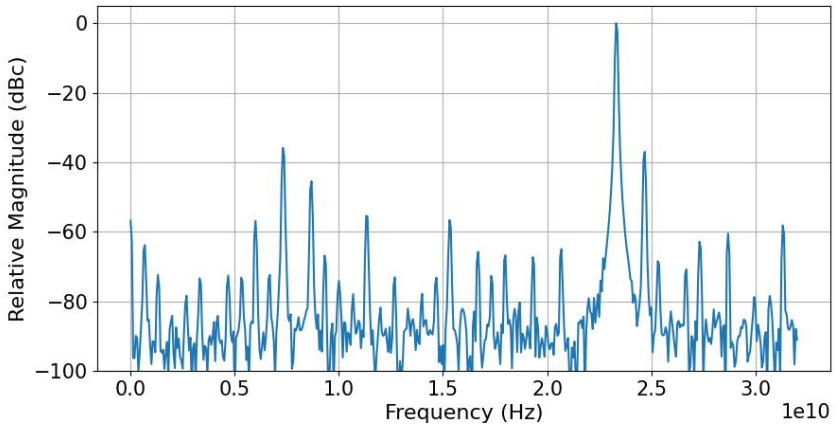

Figure 4.8: Limit test of clock generation network. Input frequency at $31.975GHz$.

Limit Testing Clock Generation Network

The clock generation is very vital for a time-interleaved network to function. Therefore, the clock generation network was limit tested. The input frequency to the clock generation network, assumed being from an on-chip PLL, was varied with a deviation of maximum $\pm 200MHz$ with increments of $25MHz$ and $12.5Mhz$.

Looking at Figure 4.11 and Figure 4.12 unrealistic results are present. To understand these results, it is required to take a further look into the generated clock signals when the input frequency is shifted. As per Figure 4.13, it is noticeable that with a drifted frequency to $31.8GHz$, the clock signals still look relevant, however, shifted in time compared to that of the $32GHz$ input clock. Since the output is sampled according to a $32GHz$ clock division, when the clock drifts, the outputs are sampled at the wrong time. This includes other frequency artifacts that are not accurate, and explains why the results look they do in Figure 4.11 and 4.12.

4.1.3 Complete System with Non-ideal Clock Generation

Here, the whole system, clock generation and TI network, is combined and simulated. Presented are comparative measurements between the ideal and non-ideal systems as well as more in depth measurements and analysis of the non-ideal network.

Signal Propagation Through One Channel

An objective verification of the functionality of the TI network with the clock generation network is a signal propagation from RF signal to ADC input, which can be seen in Figure 4.14 and 4.15. Noticeable from the graphs are the clock skew

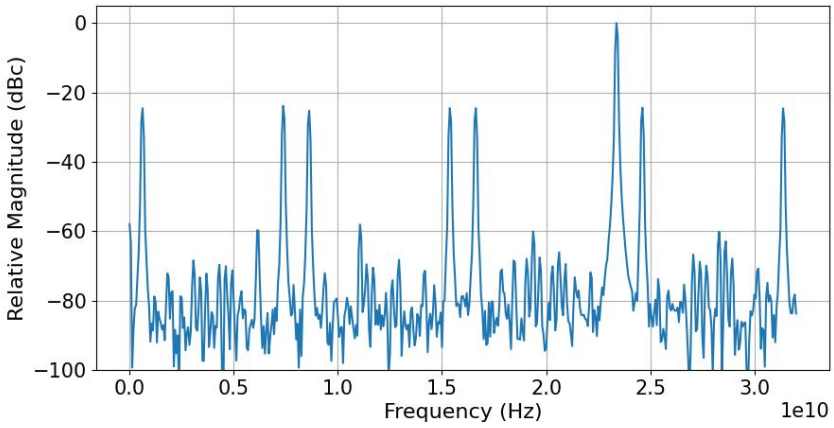

Figure 4.9: Limit test of clock generation network. Input frequency at $31.9GHz$.

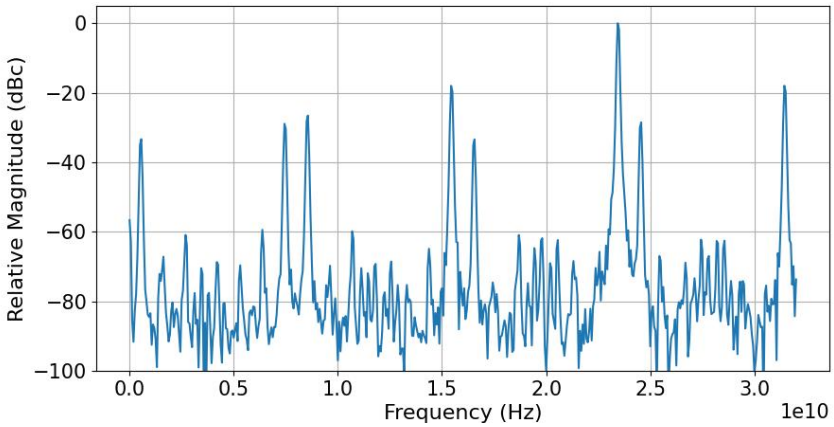

Figure 4.10: Limit test of clock generation network. Input frequency at $31.8GHz$.

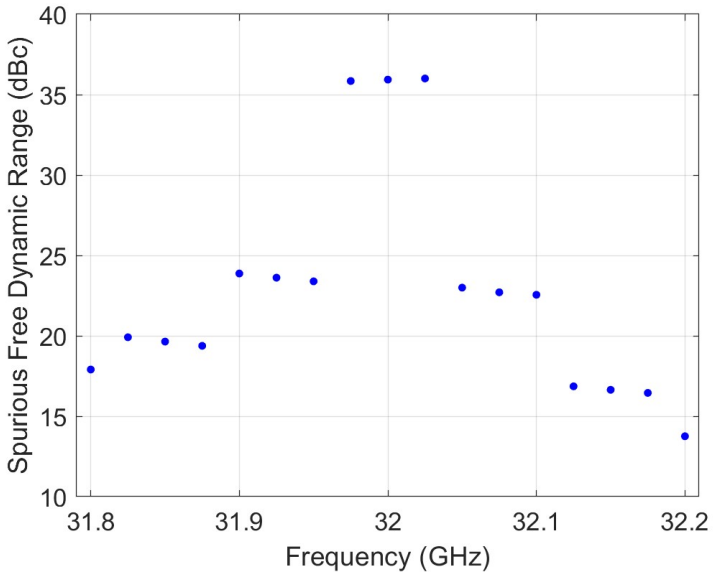

Figure 4.11: SFDR of sampled output with varying clock generation input frequency, step size of $25MHz$.

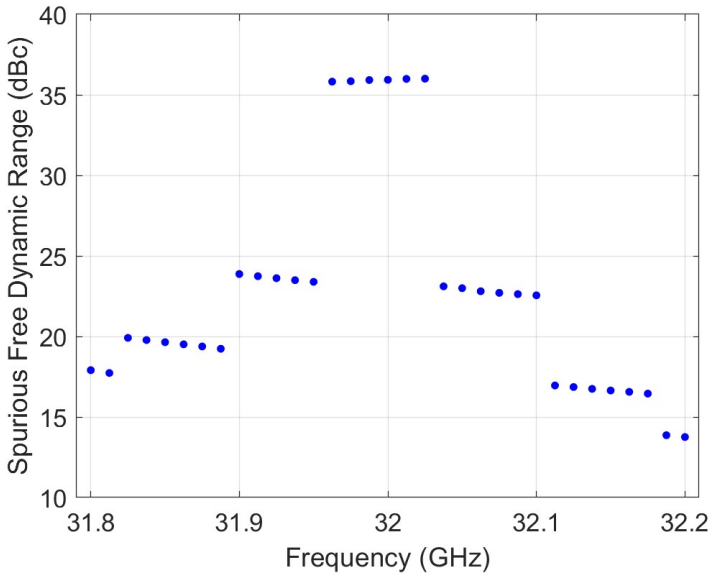

Figure 4.12: SFDR of sampled output with varying clock generation input frequency, step size of $12.5MHz$.

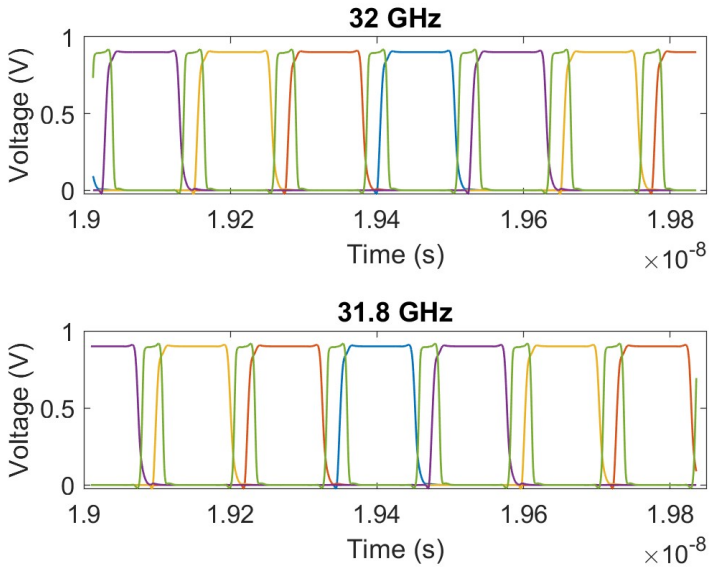

Figure 4.13: SFDR of sampled output with varying clock generation input frequency, step size of $12.5MHz$.

effects, as the buffered signal is varied depending on load. This is an observable mismatch occurring. Comparing the 1^{st} and 2^{nd} tracking it is obvious that the 1^{st} rank suffers from very low track time, $T_{T/H,time} = 31.25ps$, due to the input frequency.

FFT

In the following figures, sampled outputs for some frequencies and SFDR are presented.

With the implementation of the non-ideal clock generation network several spurs are prevalent. These added spurs are due to sampling time skew. Comparing Figures 4.2 and 4.16, which have the same input frequency, extra spurs can be observed at $f_1 = 13.34GHz$, $f_2 = 18.7GHz$, and $f_3 = 29.31GHz$. This links back to Equation 3.12. The other mismatch spurs, gain, bandwidth, and offset, are not present due to the ideality of the TI network.

Noise in TI Network

In this section, noise is added to the time-interleaved and clock generation networks. The noise that is simulated in the circuit is phase noise and transistor noise, which includes thermal noise and flicker noise.

Comparing Figures 4.20 and 4.21 to the corresponding frequencies without noise, Figures 4.16 and 4.18, the noise floor has increased noticeably. This sets a

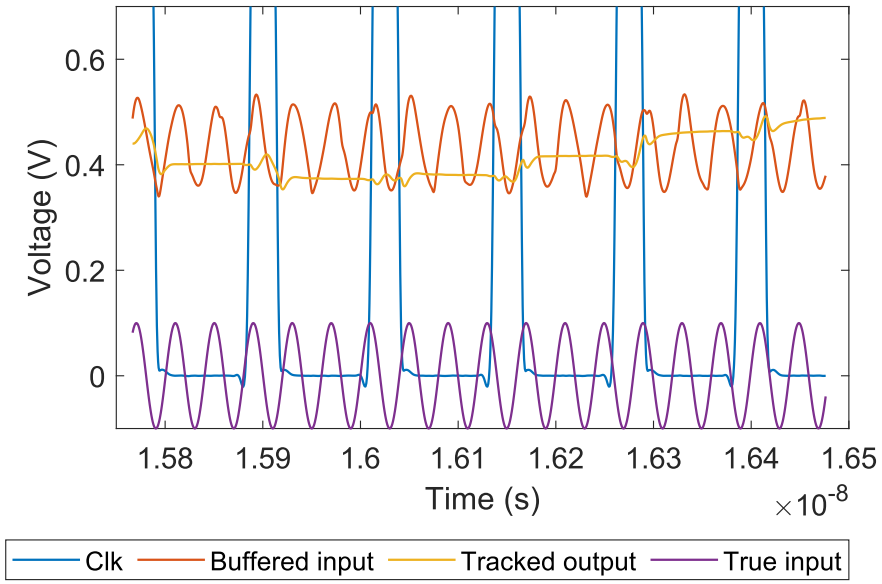

Figure 4.14: Signals that are related to the 1^{st} rank T/H. Input RF frequency at $25.0625GHz$.

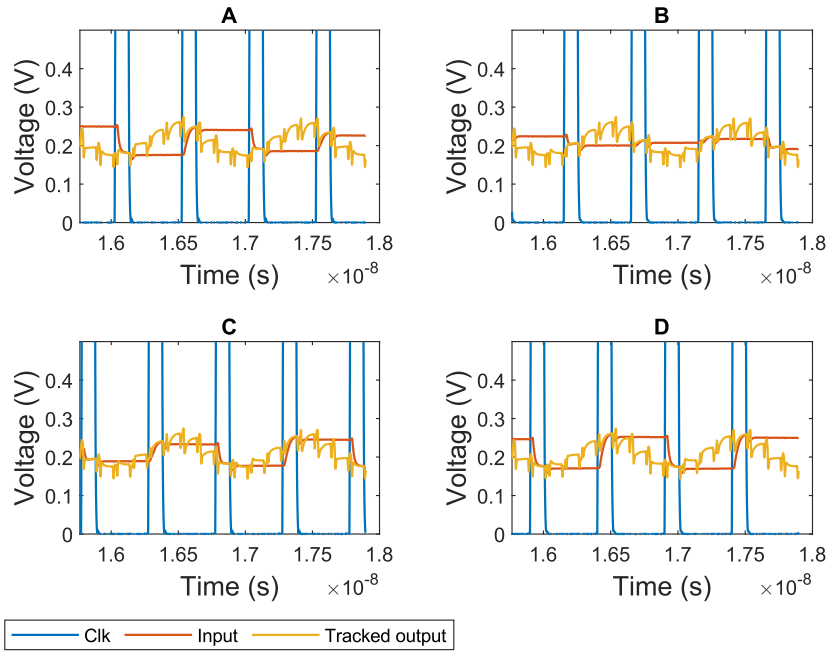

Figure 4.15: Signals that are related to the propagation of RF signal after the 1^{st} rank T/H. Input RF frequency at $25.0625GHz$.

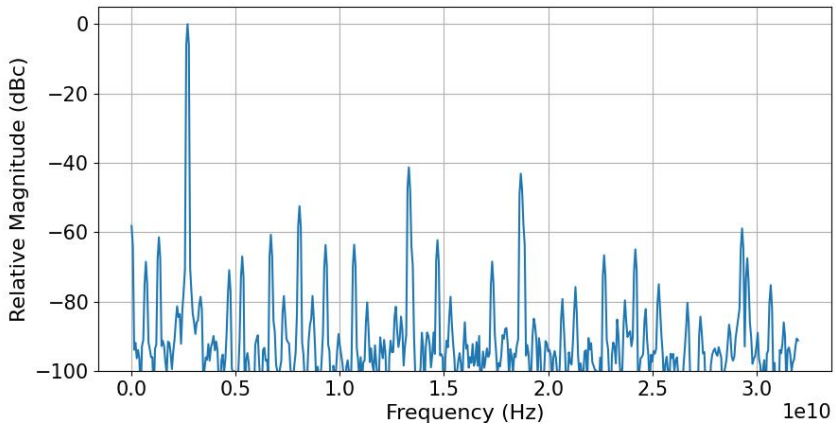

Figure 4.16: FFT of sampled output with input frequency at $f_{in} = 2.6875GHz$. Non-ideal clocking.

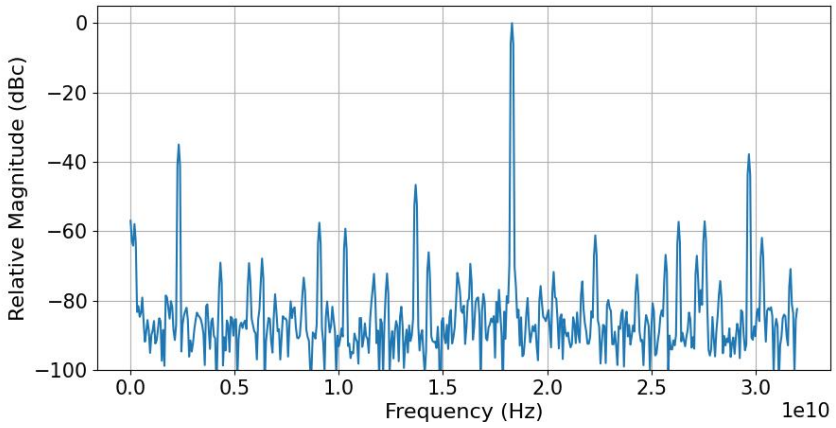

Figure 4.17: FFT of sampled output with input frequency at $f_{in} = 18.3125GHz$. Non-ideal clocking.

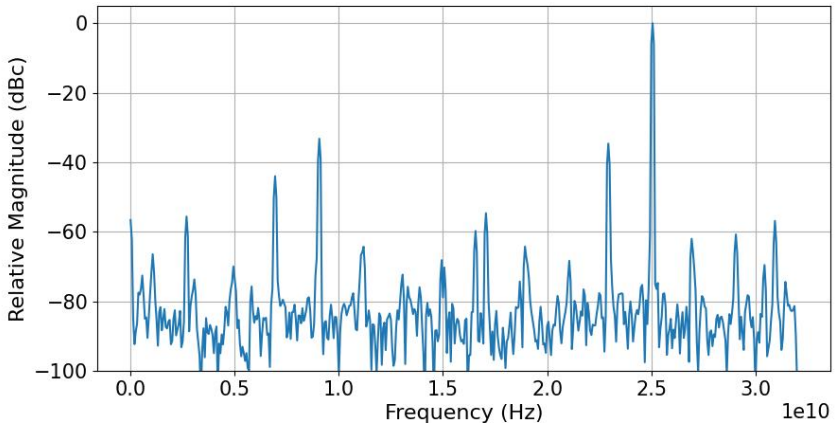

Figure 4.18: FFT of sampled output with input frequency at $f_{in} = 25.0625GHz$. Non-ideal clocking.

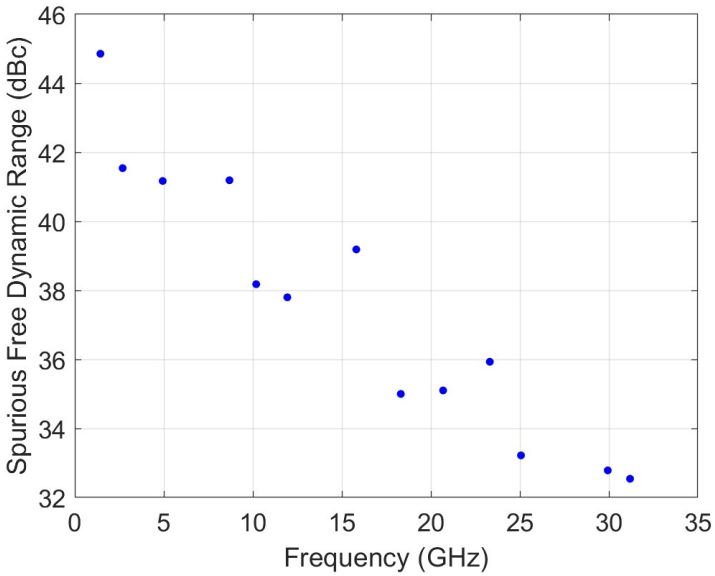

Figure 4.19: SFDR of the non-ideal clocked TI network.

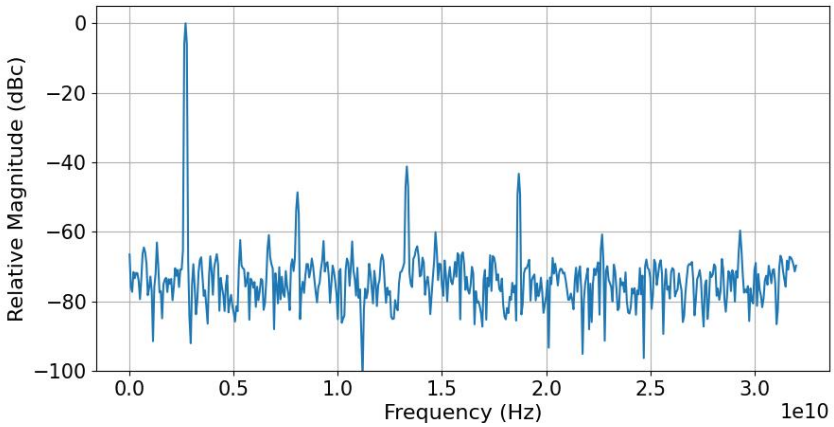

Figure 4.20: FFT of sampled output with input frequency at $f_{in} = 2.6875GHz$. Non-ideal clocking with noise.

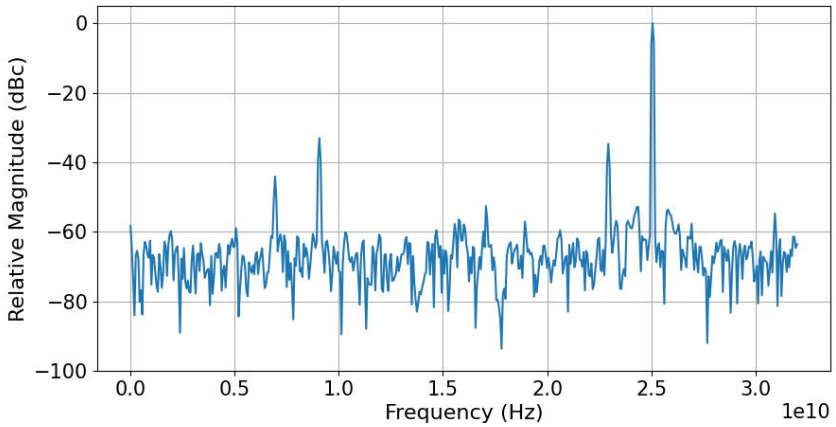

Figure 4.21: FFT of sampled output with input frequency at $f_{in} = 25.0625GHz$. Non-ideal clocking with noise.

criterion for the input stages before the time-interleaving network to have lower input noise than the generated circuit noise.

In both SFDR and SNR figures, Figure 4.22 and Figure 4.23, a downward trend can be observed with increasing frequency. This is a reasonable result given that the noise is a constant addition to the sampled signal. Higher frequency signals have a lower number of sampled values per period, which means that the noise has a greater degenerative effect.

Phase Noise in Clock Dividers

An effort was made to determine the relative performance of the clock dividers with phase noise. This was unfortunately not possible due to non converging pss simulations. The most likely factor to this is that the CML implementation has some self oscillating behavior, which makes it difficult for the clock system to find a stable state. Due to limited time, redesigning the system for a converging periodic steady state (pss) was not achieved at the end of this thesis work.

Monte Carlo Simulation

The system was tested with process variation to evaluate the stability. This includes transistor variations, which gives rise to mismatches in the channels. In Figures 4.24 and 4.25 two FFT graphs can be observed. In these figures several more spurs have appeared. These spurs are bandwidth, offset, and gain mismatches. For example, in Figure 4.24, the spur located at $10.664GHz$ is a gain mismatch spur, the one located at $13.331GHz$ is a bandwidth mismatch spur, and the spur at $8GHz$ is an offset mismatch. Several of the other spurs are also one of gain, offset, skew, or bandwidth. The same applies to Figure 4.25 where the spurs can be given a specific contributor.

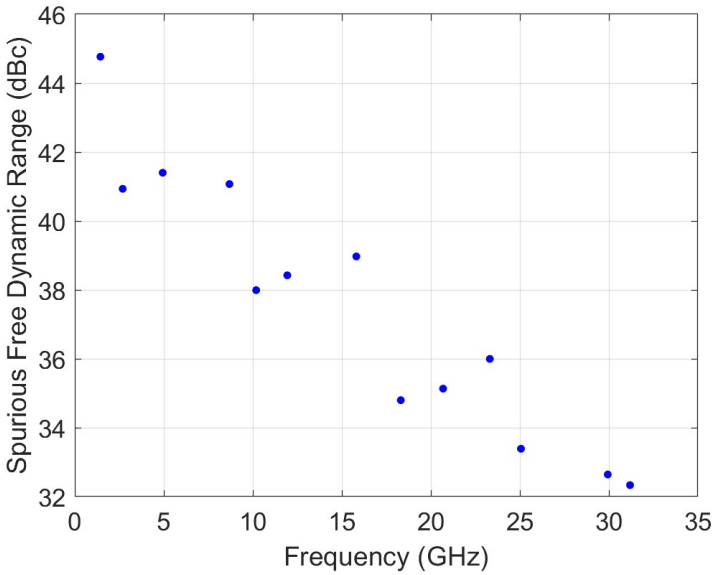

Figure 4.22: SFDR of the non-ideal clocked TI network with noise.

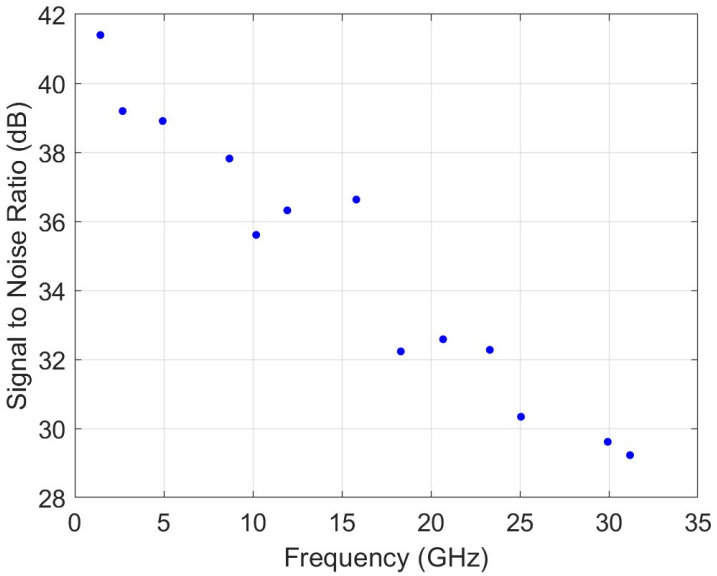

Figure 4.23: SNR of the non-ideal clocked TI network with noise.

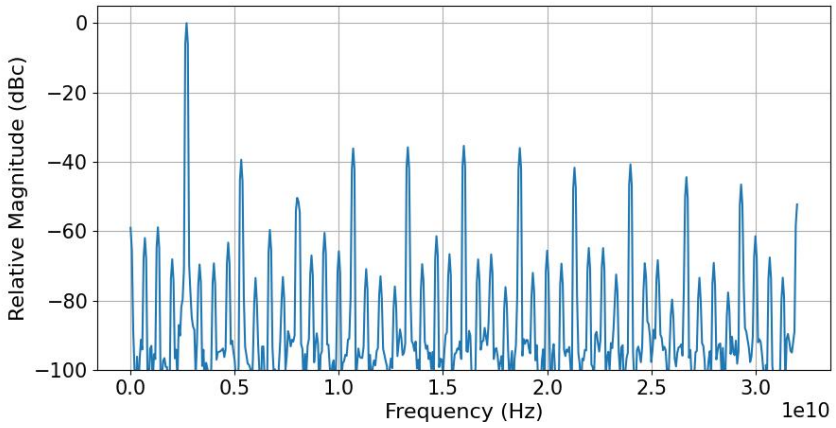

Figure 4.24: Monte Carlo simulation with the input frequency of $f_{in} = 2.6875GHz$.

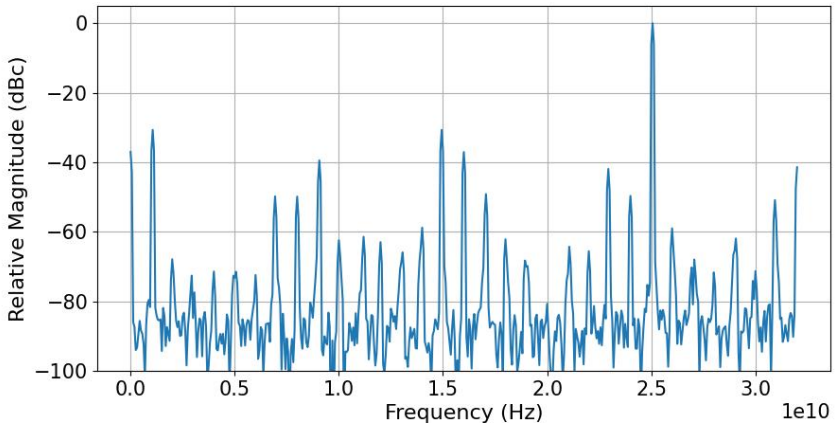

Figure 4.25: Monte Carlo simulation with the input frequency of $f_{in} = 25.0625GHz$.

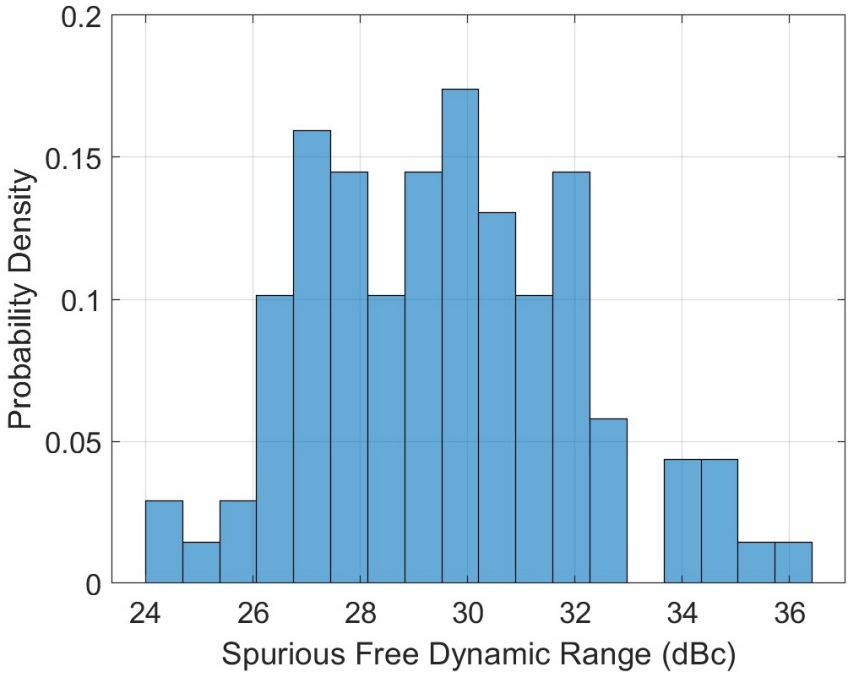

Figure 4.26: SFDR at the frequency of $25.0625GHz$ for 100 Monte Carlo simulations.

In Figure 4.26 a histogram of one hundred Monte Carlo simulations can be observed. In the figure there is a good indication of a bell curve distribution centered around a median SFDR of $30dBc$. This result, from one hundred Monte Carlo simulations, indicates a stable system where a functional time-interleaved network with a clock generation network functions regardless of process variations.

4.1.4 Power Consumption

The total power consumption was measured in stable state and was determined to be $484mW$. Comparing this to another research paper [5] using a smaller technology node, achieving power consumptions of $227mW$ excluding ADCs, the presented design has a higher power consumption. However, comparing to a similar node as in [20], with power consumption of $753mW$ excluding ADCs, comparable power consumption can be observed when considering the difference in sampling rate.

Chapter 5
Conclusion

The goal of this thesis was to construct a time-interleaved network with a sampling rate of $64GS/s$ intended for the FR3 range, $7.125GHz$ to $24.25GHz$. A higher sampling rate was implemented then required because of easy of design with a base 2 interleaving network and end stage ADCs having a sampling rate of $2GS/s$. A time-interleaved network with buffers and T/Hs to distribute samples to ADCs. In addition, a clock generation network creates the sampling clocks for the 1^{st} and 2^{nd} rank T/Hs.

Achieving a power consumption of $484mW$ is comparable to the state of the art interleaving networks. Since the main goal of the work was not focusing on power consumption this is a great addition to the thesis results. Having a high SFDR for the FR3 band was achieved however, with more time and optimization it could have been improved further. With the addition of spurs from both clock generation and process variation, the dynamic range is still effective up to very high frequencies. Due to the way the samples are distributed along the channels, the collection of data was very tedious. It would be interesting to verify the network with the addition of end stage ADCs.

5.1 Future work

For future work there are several different paths. Firstly, in our opinion the next stage is the addition of end stage ADCs. This would complete the analog front-end for the direct RF sampling circuit. The suggestion of ADC architecture for a TI network is the SAR ADC as it has a low area and power consumption, as well as smaller input capacitance. This smaller capacitance would ease the design of the T/Hs. Considering the additional area that comes with 32 channels, with each having an end stage ADC, the total area increases rapidly. With a smaller input capacitance to the ADCs, the strain on the time interleaved network decreases.

Secondly, it is possible to expand the network for even higher sampling rate, possibly including the FR2 band.

Thirdly, enabling on and off switching of subsequent channels would allow for a varying sampling rate up to $64GS/s$. This, to achieve a lower power consumption when looking at lower parts of the FR3 band, where the higher sampling rate is negligible. Lastly, adding a digital or analog calibration circuit would be beneficial in the removal of spurs, leading to an improved SFDR.

Further investigate in to the clock generation network would be needed. As of the end of the project a stable state for the CML circuit was not achieved.

References

[1] "Digital beamforming for mobile devices," white paper, BeammWave, Sweden. Accessed: 2026-06-16.

[2] H. Nyquist, "Certain topics in telegraph transmission theory," *Transactions of the American Institute of Electrical Engineers*, vol. 47, no. 2, pp. 617–644, 1928.

[3] J. Heel, H. S. Bindra, S. M. Louwsma, A. Dezzani, and B. Nauta, "A 12.8-gs/s time-interleaved sub-sampling adc front end with 38-ghz input bandwidth and >39-db sndr for 1–32 ghz in 22-nm fdsoi," *IEEE Journal of Solid-State Circuits*, vol. 60, no. 12, pp. 4321–4335, 2025.

[4] W. Black and D. Hodges, "Time interleaved converter arrays," *IEEE Journal of Solid-State Circuits*, vol. 15, no. 6, pp. 1022–1029, 1980.

[5] Y. Zhang, M. Zhang, Z. Wu, Y. Zhu, R. P. Martins, and C.-H. Chan, "A 72-gs/s 9b time-interleaved pipeline-sar adc achieving 55.3/49.3-db sfdr at 20-ghz/nyquist inputs in 16-nm finfet," *IEEE Journal of Solid-State Circuits*, vol. 60, no. 12, pp. 4515–4531, 2025.

[6] G. Manganaro, "An introduction to high sample rate nyquist analog-to-digital converters," *IEEE Open Journal of the Solid-State Circuits Society*, vol. 2, pp. 82–102, 2022.

[7] Y. Duan and E. Alon, "A 12.8 gs/s time-interleaved adc with 25 ghz effective resolution bandwidth and 4.6 enob," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 8, pp. 1725–1738, 2014.

[8] A. Ramkaj, M. Perrott, B. Haroun, and B. Murmann, "High-linearity high-bandwidth (>20ghz) th front ends using active bootstrapping and heterogeneous sige/cmos circuit co-design," in *2023 IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1–5, 2023.

[9] A. S. Yonar, P. A. Francese, M. Brändli, M. Kossel, T. Morf, J. E. Proesel, S. Rylov, H. Ainspan, M. Cochet, Z. Deniz, T. Dickson, T. Beukema, C. Baks, M. Beakes, J. F. Bulzacchelli, Y.-H. Choi, B.-J. Yoo, H. Ahn, D.-H. Lim, G. Kang, S.-H. Park, M. Meghelli, H.-G. Rhew, D. Friedman, M. Choi, M. Soyuer, and J. Shin, "An 8-bit 56gs/s 64x time-interleaved adc with bootstrapped sampler and class-ab buffer in 4nm cmos," in *2022 IEEE Symposium*

on VLSI Technology and Circuits (VLSI Technology and Circuits), pp. 168–169, 2022.

[10] W. Xiaofeng, L. Hongxia, S. Li, H. Yue, L. Di, and H. Shigang, "A bootstrapped switch employing a new clock feed-through compensation technique," *Journal of Semiconductors*, vol. 30, p. 125007, dec 2009.

[11] H. Agarwal and A. Rana, "Front end track and hold circuit for high speed analog to digital converters," in *2012 International Conference on Communication Systems and Network Technologies*, pp. 785–789, 2012.

[12] Y. Zhu, T. Liu, S. K. Kaile, S. Kiran, I.-M. Yi, R. Liu, J. C. G. Diaz, S. Hoyos, and S. Palermo, "A 38-gs/s 7-bit pipelined-sar adc with speed- enhanced bootstrapped switch and output level shifting technique in 22-nm finfet," *IEEE Journal of Solid-State Circuits*, vol. 58, no. 8, pp. 2300–2313, 2023.

[13] R. Darraji, R. Barrak, C. Rebai, A. Ghazel, Y. Deval, and F. Ghannouchi, "Track and hold circuit design and implementation in 65 nm cmos technology for rf subsampling receivers," in *2008 15th IEEE International Conference on Electronics, Circuits and Systems*, pp. 1249–1252, 2008.

[14] F. Yuan, "Design techniques for sample-and-hold with bootstrapping in low-power sar adc," in *2024 22nd IEEE Interregional NEWCAS Conference (NEWCAS)*, pp. 293–297, 2024.

[15] N. Kurosawa, H. Kobayashi, K. Maruyama, H. Sugawara, and K. Kobayashi, "Explicit analysis of channel mismatch effects in time-interleaved adc systems," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 48, no. 3, pp. 261–271, 2001.

[16] R. Levinger, J. Kadry, and A. Bechtold, "A 50 ghz 2 mw inductor-less frequency divider with back-gate tuning achieving a locking range of 160

[17] M. Vigilante and P. Reynaert, "A 25–102ghz 2.81–5.64mw tunable divide-by-4 in 28nm cmos," in *2015 IEEE Asian Solid-State Circuits Conference (A-SSCC)*, pp. 1–4, 2015.

[18] N. Saquib and M. M. Hella, "A 75–110 ghz wide band dynamic latch frequency divider in 22nm fdsoi technology," in *2025 IEEE 68th International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 932–935, 2025.

[19] Geum-young), "Differential output tspc d-type flip-flop and frequency divider using the same," Feb. 2007.

[20] C. Rudorf, N. Lotfi, S. Linnhoff, E. Wittenhagen, Kesten, and F. Gerfers, "A nyquist-rate 128 gs/s 6-bit 64x time-interleaved sar adc in 22nm fd-soi," in *2025 IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1–5, 2025.

Appendix A
Extended Material

A.1 Calibration

Zhang et al. [5] have done a thorough investigation of the time-interleaved network where they have taken into account mismatch errors in every decision. They have implemented a calibration technique that during system running mitigates, skews, gains, and offset spurs.

The calibration of a TI network can be done both analog and digitally. As well as in the foreground and background. Foreground calibration is done with a known input signal that the chip can than use to know where adjustments to the circuit has to be done. This is done before the chip is sold and then also when the circuit is started, but less extensive. Background calibration is done continuously during operation. Changes that can occur during regular operation are for example, temperature variations.

Analog calibration is done with analog circuitry "sensing" the non-idealizes on the chip where they happening. With this sensing circuitry, the mismatch can be either corrected or canceled from the TI output. This calibration is done in the background.

Digital calibration is done by inspection of the output. It is done in the background but can also be implemented in the foreground[6].

A.1.1 Randomize The Sampling of The ADCs

Mismatch mitigation is maybe not always be an option or the calibration techniques is not enough to completely remove the effects. To further reduce mismatch spurs an additional mitigation technique is possible, randomization.

Since the mismatch spurs originate from a mixing of periodic errors in the channels, breaking this periodicity can mitigate the problem. This would make the spurs irregular and therefore improve performance[6].

A.2 Other Direct RF Sampling Options

Other researchers have taken another approach towards direct RF sampling[3]. Instead of pushing for higher sampling rates to increase the bandwidth in the first Nyquist region, a reduction of SNDR in higher Nyquist zones has been targeted,

see Figure 2.2. Changing focus from increasing sampling rates to a reduction of SNDR instead creates a lower demand on power consumption and calibration, as the interleaving network has reduced in size. Reducing SNDR in higher nyquist zones means that undersampling can be utilized, where the higher frequency signals are aliased. This method sets high criteria on LNA and other analog front-end blocks to reduce noise and distortion contributions.