Key analog/RF blocks for a programmable broadband actuator architecture

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Abstract

In modern telecommunications, the ever increasing demands on signal bandwidth with the adoption of Millimeter Wave (mm-W) frequency bands for the Fifth-Generation (5G) standard make ensuring Power Amplifier (PA) linearity, while maintaining efficiency, a major challenge in the design of Transmitter (TX) circuits. As Digital Pre-Distortion (DPD) linearizers become too power hungry for wide-band applications, various Analog Pre-Distortion (APD) techniques have been explored as alternatives. However, the applicability of these is typically limited to a single or a narrow range of PA topologies. This work presents a novel concept for a combined DPD and APD system with a tunable transfer function for the APD allowing for digital control by the DPD based on the PA distortion characteristic. As a result power consumption can be reduced compared to pure DPD and the system may be utilized to linearize a wide range of different PAs.

Preface

This thesis is for the masters degree in embedded electronics engineering at Lund University. The work was carried out at Ericsson AB in Lund who provided all the necessary equipment and resources for the project as well as valuable knowledge and a learning compatible work environment. I would like to thank the project supervisors at Ericsson AB, Rehamn Akbar and Fabien Mesquita, as they have provided valuable guidance over the course of this work. Also I would like to extend my gratitude to Daniele Mastantuono, manager of the Hardware Design Unit for Integrated Radio Systems of Ericsson research in Lund. Finally I would like to thank the university supervisor at LTH, Henrik Sjöland.

Popular Science Summary

Wireless telecommunication, a facet of modern life which has completely altered the way human society functions. The simple ability to communicate across the globe almost instantaneously can be said to have redefined modern life. We are now able to contact friends and family whenever we wish, work remotely, communicate with strangers we would have never have been able to interact with were it not for the existence of these technologies, among numerous other things which would have been unimaginable to the average person living 50 years ago. This sudden paradigm shift in our lives has been enabled by the rapid development and mass adoption of modern communication technologies, which is still progressing as fast as ever at the time of writing.

A crucial concern in this field is ensuring that the information, transmitted through the air in the form of electromagnetic waves, is recognizable enough to be processed at the receiving end. Electromagnetic waves have two main properties: frequency and power. The frequency describes the speed at which a wave oscillates, that is, how many "peaks" and "valleys" appear in the wave over the course of 1 second. Power, on the other hand, is defined as the amount of energy contained in a wave, quite literally how powerful it is, meaning how tall the "peaks" and how deep the "valleys" are. Advantage is taken of both these quantities to ensure that information travels properly.

The frequency of a wave allows for it to be distinguished from radiation at other frequencies. Therefore, to make certain that signals from different devices do not interact or "mix", so called frequency "bands" are allocated for each signal, defining the frequencies it is allowed to occupy. This is typically referred to as the signal bandwidth, the width of its frequency band. Digital information is made up of bits and in general any useful piece of data contains multiple thousands of these. If the bandwidth of a signal is wide it can carry a large amount of information in a short amount of time, which enables fast communication. Consequentially, as the field develops and the demands on speed and the quantity of data to be transmitted increase (high quality video streaming for example), a central goal becomes to produce devices which are able to handle wider signal bandwidths.

The signal carrying this information must be powerful enough to travel the needed distance and not be drowned out by disturbances caused by the radiation which is ever present at all frequencies, known as "noise". A receiver system will always pick up this noise and the signal power must be high enough to ensure that the data is detectable. For this reason, the systems within our electronics which are responsible for transmission contain a component known as a power amplifier.

The power amplifier is responsible for amplifying the signal power before it is transmitted through the air. Naturally, since energy cannot be generated from nothing, a certain amount must be fed into these components. Some of this energy will be lost in the form of heat instead of being used for the intended purpose, a limitation of all electronics. In transmitter systems the power amplifiers are generally the most significant contributors to the overall power consumption. Additionally, the power efficiency of these devices will increase for stronger signals. Essentially, feeding a more powerful signal into the amplifier would make it more efficient, meaning that a larger part of the invested energy is converted to useful output signal compared to that wasted as excess heat. An issue, however, is the fact that power amplifiers distort stronger signals more, making them unusable after a certain point, setting a limit on how effectively the device may be utilized.

To remedy the issue of distortion caused by power amplifiers, while keeping efficient operation, a widely used technique is something called pre-distortion. The input signal is deformed in a way opposite to that which it would experience passing through the amplifier. As a result the distortion of the amplifier shapes the signal back into its original form and all information is preserved. The typical way this is done is via digital pre-distortion, deforming the signal based on mathematical algorithms applied in the digital domain. The advantage here is that the pre-distortion may be manipulated in any way desirable as any function may be applied to the digital signal. A core disadvantage is the fact that as the signal bandwidth increases, the digital circuitry must operate at faster rates while performing complex calculations, therefore consuming more energy. The entire goal of this technique is to make a more efficient system, but after a certain point digital pre-distortion becomes an ineffective solution.

For this reason a method known as analog pre-distortion has been explored for use at high signal bandwidths to save power. What is meant by analog here is that the processing is done on the signal after it has been converted from digital to analog form. This has the advantage of the circuitry not being required to perform any digital calculations, rather the pre-distortion is done by shaping the form of the analog signal directly. Unfortunately, the main benefit is also a major downside as analog circuitry cannot be easily reprogrammed and can typically only be applied to a single power amplifier design, good for highly specific use cases like satellite technologies, but making it less suitable for mass adoption in everyday consumer electronics.

The underlying idea behind the work done for this thesis is the possibility of combining these two methods in a sort of digital and analog hybrid pre-distortion system which would keep the advantage of re-programmability while retaining the increased efficiency of analog processing. More specifically, the thesis work revolves around designing the core block of the analog part for this system, which shapes the signal and is controlled by the digital component. The main challenge to be overcome is the design of analog circuitry fast enough to handle high bandwidth signals.

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List of Abbreviations

5G	Fifth-Generation
BB	Baseband
mm-W	Millimeter Wave
AM-AM	Amplitude-to-Amplitude
CMOS	Complementary Metal Oxide Semiconductor
DPD	Digital Pre-Distortion
APD	Analog Pre-Distortion
PD	Pre-Distortion
FDSOI	Fully Depleted Silicon-On-Insulator
MOSFET	Metal-Oxide-Semiconductor Transistor
Op-Amp	Operational Amplifier
PA	Power Amplifier
PAPR	Peak-to-Average Power Ratio
RF	Radio Frequency
TX	Transmitter
IM3	3rd order Inter-Modulation components
I/Q	In-phase and Quadrature-phase
BW	Bandwidth
FB	Feedback
CM	Common Mode
CMFB	Common Mode Feedback
GBW	Gain Bandwidth product
SR	Slew-Rate
$\mathbf{V_{DS}}$	Drain-to-Source Voltage
$\mathbf{g_m/I_D}$	Transconductance Efficiency
$\mathbf{I_D/W}$	Drain Current Density
$\mathbf{I_D}$	Bias Drain Current
$\mathbf{V_{GS}}$	Gate-to-Source Voltage
$\mathbf{V_{OV}}$	Overdrive Voltage
$\mathbf{g_m}$	Small Signal Transconductance
PDK	Process Design Kit
PM	Phase Margin
RHP	Right Half Plane
LHP	Left Half Plane
L	Channel Length
W	Total Gate Width
OL	Open-Loop
CL	Closed-Loop
$\mathbf{Y_{12}}$	Reverse Transfer Admittance Parameter

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Chapter 1
Introduction

With the ever growing requirements for speed in modern telecommunication and the widespread adoption of the 5G standard, the high frequency 5G mm-W bands, also referred to as Frequency Range 2 (FR2), have become increasingly attractive. The wide spectrum available in these bands enables the use of wide-band radio signals for high-data-rate and high capacity communication [1].

The hardware driving telecommunication systems for these must therefore be designed with wide-band operation in mind. A key component required at the end of the TX chain is the PA, ensuring amplification of the signal power to a level sufficient for transmission. With modern communication standards utilizing modulation schemes demonstrating high Peak-to-Average Power Ratio (PAPR) a critical limit on these systems becomes the distortions introduced by PAs at higher signal levels. Due to this behavior PAs must be operated at power back-off degrading the overall system efficiency [2].

A common solution for mitigating these issues in modern circuits is known as PA linearization. This technique reduces the need for operation at power back-off by removing (or reducing to acceptable levels) the signal distortions introduced by the PA. Several methods for linearization have been demonstrated but the most commonly utilized today is pre-distortion linearization [3]. This form of linearization introduces a system in the TX chain which compensates for distortions by "pre-distorting" the signal in an inverse way to that of the PA. The overall effect is that of a more linear signal (ideally undistorted) at the output of the PA [4].

Today, pre-distortion is most commonly implemented in the digital domain, known as DPD. This method introduces a digital component to the signal path in Baseband (BB), before digital-to-analog conversion, along with a feedback system from the PA output, to pre-distort the signal. As PAs distortions generate out-of-channel components [5], DPD blocks must be able to generate pre-distorted signals at several times the BB Bandwidth (BW) [4]. Consequently, DPD circuits demonstrate excessive power consumption for high BW signals, unacceptable for the aforementioned wide-band radio signals [4]. For such applications a possible pre-distortion technique is known as APD in which the signal is pre-distorted in the analog domain rather than the digital [3], [4], [6].

Much work has been done on various methods for APD linearization. [7], [8] and [9] demonstrate Complementary Metal Oxide Semiconductor (CMOS) PAs with built-in APD linearization using cold-FETs, wherein Metal-Oxide-Semiconductor Transistors (MOSFETs) with a 0 V Drain-to-Source Voltage (V_{DS}) serve as passive components achieving the required Pre-Distortion (PD) for the PA. This passive APD has the ad-

vantage of reducing overall system complexity since it requires only one additional component in the signal path [9]. In [10] the APD is performed by a separate component to the PA although this design is specific to the architecture of the PA to which it is applied. All of these examples can only be applied to the PA for which they were designed and are thus application specific.

[4] shows a stand-alone APD component which is more generic and applicable to a wider range of PAs. However, this design is limited to E-band mm-W PAs. This is a consequence of the circuit being designed to act on the signal in the Radio Frequency (RF) domain. For linearizers to cover the memory effects of the PA distortion, time delay elements are necessary in the signal path. These elements will depend on the frequency at which the APD circuit operates [11]. Achieving a compatibility for the APD component with a wider range of PAs, independent of the RF at which the PAs operate may be possible by pre-distorting the signal in the BB domain instead. This idea will be further elaborated upon in chapter 2 and serves as a key concept behind the thesis project.

The work done in this thesis will consist of the design of an analog circuit serving to realize a tunable gain expansion transfer function as part of an APD component. This component is intended to pre-distort the signal in the BB frequency domain, before signal up-conversion to RF, making it independent of the linearity profile of the PA as well as its frequency of operation. Such a combination of tunable gain expansion and RF independence would allow for the system to be applied to a wide range of PAs. The scope of this thesis does not include any fabrication and the evaluation of the design will be limited to circuit simulations.

Chapter 2 will define the project starting with an explanation of the main concepts behind the work, moving on to the proposed circuit design and the necessary performance specifications required for it to achieve the desired functionality. Chapters 3 and 4 will cover the design of the Op-Amp and FB network which are the main two constituent blocks of the circuit, making up the two phases of the thesis work respectively. Chapter 4 will also present the simulation results for the finalized design and chapter 5 will serve as a brief conclusion on the project.

The necessary CAD tools were supplied by Ericsson AB; Cadence Virtuoso and ADE for circuit simulations. The work was carried out in the 22nm Fully Depleted Silicon-On-Insulator (FDSOI) CMOS technology. Office space and computers were also provided by Ericsson AB.

Chapter 2
System Definition and Specifications

This chapter will serve to define the circuit design goals for this thesis. Initially a more in-depth explanation of the decision to linearize the signal in BB will be given in section 2.1, moving on to the definition of the desired piecewise linear transfer function and providing a brief schematic overview of the circuit proposed in section 2.2. Further on, section 2.3 shows the process by which the design was initially modeled with the purpose of theoretically validating the proposed circuit and section 2.4 will define the necessary specifications which it must meet to achieve the desired functionality.

2.1 Combined Digital and Analog Baseband Linearization

The fundamental idea behind the work in this thesis is to achieve partial APD by cascading with the DPD system in the BB domain. This would introduce the added advantage of making the pre-distortion system independent of the PA frequency of operation, due to the signal being pre-distorted before up-conversion to RF.

Figure 2.1 gives a block diagram overview for a theoretical TX system which would incorporate the signal expansion in BB, before the up-conversion mixers.

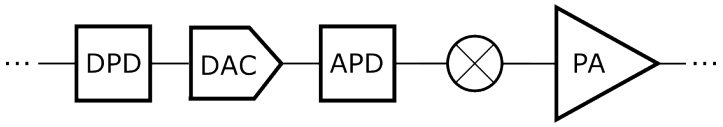


Figure 2.1: Block diagram showing proposed system with BB linearization

This proposed BB linearization, along with making the circuit compatible with a wider number of PAs, also has the advantage of removing the need for signal splitting in RF due to the BB signal already being split into its In-phase and Quadrature-phase (I/Q) components, reducing system complexity. This signal split is desirable since it reduces the BW requirement for the circuit to half of that corresponding to the signal.

2.2 Piecewise Linear Transfer Function

The goal of this thesis is to implement a tunable component of an APD system by the use of a circuit which can alter its transfer function based on the needed gain expansion. The method of choice for this work is to implement a piecewise linear transfer characteristic for the circuit which would be digitally controllable to fit an approximation of the desired function. Figure 2.2 illustrates such a piecewise approximation of the expansion function as an example (scaled to have an initial slope of 1 such that the initial gain selected for the circuit is not lower than unity).

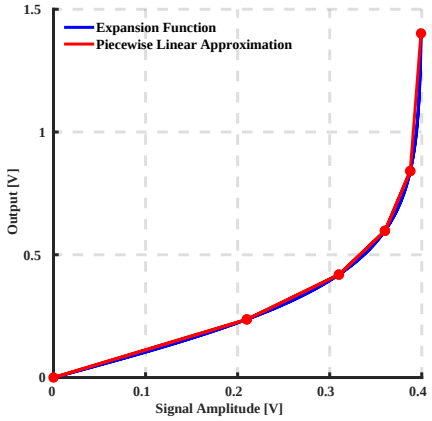


Figure 2.2: Plot showing piecewise approximation of the function with breakpoints at selected signal levels

As can be seen, the shape of the function is divided into linear segments determined by "breakpoints" placed at chosen signal amplitude levels. By altering the position of these points the circuit can be made to adapt to a variety of different signal expansions allowing for a compatibility with a wide range of PA compression characteristics.

Such a piecewise linear function would ideally be realized by switching the circuit gain at selected points of the input signal levels serving as breakpoints for the function approximation.

The proposed method of achieving the desired gain expansion is by the use of an Op-Amp with a switched resistive FB network as shown in figure 2.3.

The gain control is done by detecting the signal envelope level ($Env. = \sqrt{I^2 + Q^2}$), opening and closing switches based on this value, thereby altering the gain.

However, this implementation will not be able to exhibit a perfect piecewise linear transfer function due to the speed limitations of real components. These limitations will result in the appearance of "dead zones", i.e. regions of flat gain making the transition more of a step than a perfect switch between linear gain regions. Furthermore, the Op-Amp must demonstrate sufficient speed to keep up with a switching feedback network at the desired frequency bandwidth (800 MHz I/Q components in the worst case). Mitigating these issues will be the main challenge to be overcome during the thesis work.

The input was specified as a $0.8\,V_{PP}$ differential signal meaning the amplitude will range from 0 to $0.4\,V$. Based on the breakpoints selected in the piecewise approximation

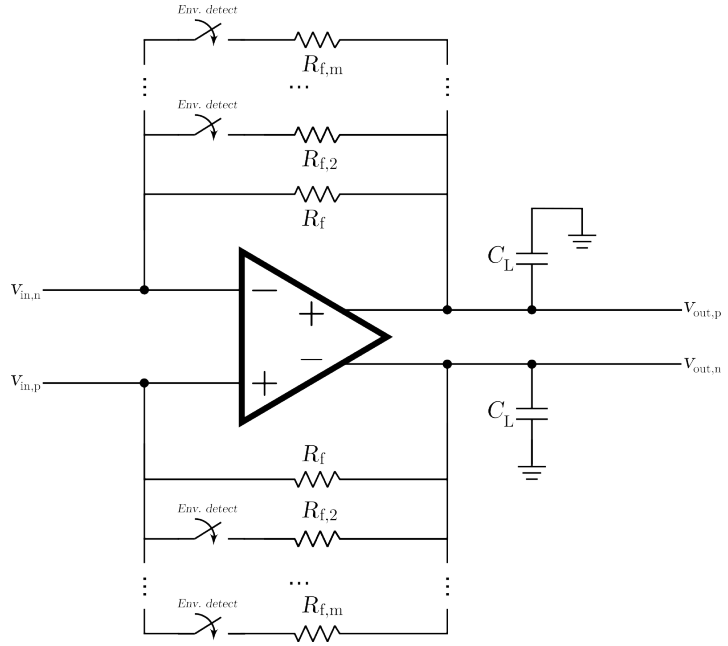


Figure 2.3: Schematic for proposed circuit to achieve piecewise linear expansion function

of the function, seen in fig. 2.2 the gain values for the circuit were determined as the slopes between these points.

Input Signal Amplitude [V]	**Linear Gain After Point**
0	$G_1 = 1$
0.21	$G_2 = 1.26$
0.31	$G_3 = 1.52$
0.36	$G_4 = 1.92$
0.3875	$G_{max} = 2.85$

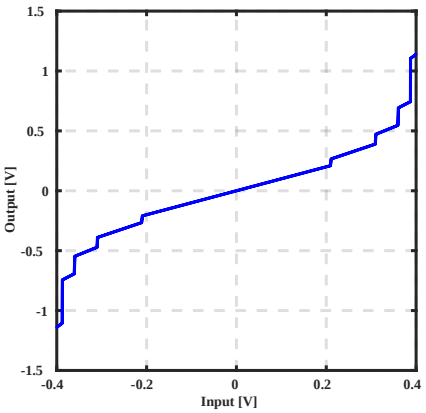
Table 2.1: Table of gain values following breakpoints at selected input signal amplitude levels

2.3 Initial circuit Modeling

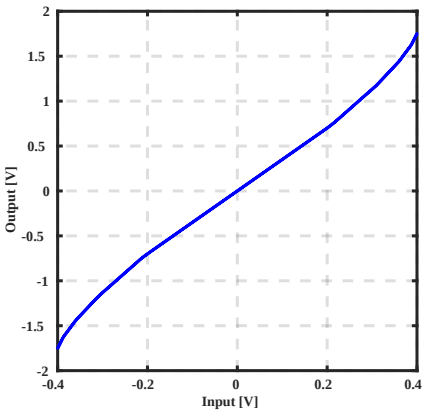
Before working on the design of real components, the circuit is verified conceptually by the use of ideal models. This is done to confirm that the idea behind the project is theoretically possible and will serve as a benchmark for comparison with the final design later on.

Initial evaluation for the design is done by simulating the circuit as an ideal com-

ponent modeled with VerilogA code. Figure 2.4a shows the simulation results of the component ideally switching between gain values at set input signal levels, demonstrating large "jumps" at the breakpoints. This is the behavior expected from an ideal Op-Amp with a switched resistive feedback applied. In figure 2.4b we observe a function which exhibits the desired piecewise linear characteristic. This is achieved by having the component shift the output voltage after a gain transition by the associated "jump" seen in figure 2.4a.



(a) Piecewise linear transfer function showing "jumps" at breakpoints



(b) Smoothed piecewise linear transfer function

Figure 2.4: Simulated transfer functions for circuit VerilogA models

Figure 2.5 shows the simulated transfer function of a switched resistive FB network applied to an ideal Op-Amp circuit model (voltage controlled current source with a resistance at the output), confirming the results from the VerilogA component models by demonstrating the same "jumps" at the switching points.

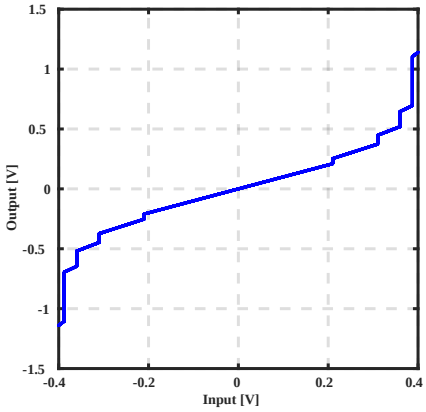


Figure 2.5: Simulation of switched resistive FB network using ideal Op-Amp model

2.4 Design Specifications

This section will serve to give a brief overview of the performance specifications which the design must fulfill. Specifications were derived based on previous internal system simulations done at Ericsson and investigations done at the start of the thesis.

The system is required to handle a *1.6 GHz* signal BW in the worst case, since the intention is to process the signal I/Q components individually the circuit may be designed to handle only half of this (*800 MHz*). To linearize the 3rd order Inter-Modulation components (IM3) components the circuit must be able to perform at three times the input BW resulting in a requirement of *2.4 GHz* for BW.

Furthermore, the input signal voltage swing requirement is given as *0.8* V_{PP}. As the design will consist of a fully differential Op-Amp this results in a need to handle *0.4* V_{PP} inputs at each end.

The circuit is initially designed and evaluated based on a piecewise-linear approximation of the desired function. Internal investigations done at Ericsson have determined the desired maximum gain of the circuit, following the final breakpoint in the piecewise-linear function, to be about 2.85 times. When considering the input swing, this sets a *2.28* V_{PP} differential output signal swing requirement, meaning each end of the circuit must handle a swing of *1.14* V_{PP} at its output. For this reason the supply voltage was set to *1.6 V* for the amplifier in order to leave some headroom for the transistors to remain in the active region.

The required *2.4 GHz* BW for the circuit along with the maximum gain of 2.85 times results in a minimum Gain Bandwidth product (GBW) specification of *6.84 GHz* for the Op-Amp. .

For the amplifier to handle a $2.4\,GHz$ and $0.57\,V_p$ signal at its output the minimal Slew-Rate (SR) must exceed $8.6\,V/ns$ based on eq. (2.1) (found as the maximum slope for a sinusoid with amplitude V_P and frequency f).

$$SR_{min} > 2\pi f V_P \tag{2.1}$$

Table 2.2 shows the design specifications. Internal evaluation determined a capacitive load ranging between *100* and *550 fF*.

Parameter	**Value**	**Summary**
f_{3dB}	2.4 GHz	3 times the worst case 800 MHz signal BW
Maximum gain (G_{max})	2.85 (linear)	Greatest slope in the transfer function
GBW	6.84 GHz	$GBW = G_{max} f_{3dB}$
V_{in} (differential)	0.8 V_{PP}	Input swing specification
V_{out} (differential)	2.24 V_{PP}	Output swing specification based on G_{max}
V_{DD}	1.6 V	Supply to handle output swing
C_L	100-550 fF	Estimated by internal evaluations
SR	8.6 V/ns	Based on signal BW and output swing

Table 2.2: Table showing design specifications

Chapter 3

Operational Amplifier Design and Performance Evaluation

This chapter will serve to cover all relevant aspects relating to the Op-Amp intended for use in the circuit shown in fig. 2.3. The specifications for the circuit are provided in table 2.2 and will dictate the main requirements. In the end, two Op-Amps were designed. These will be further evaluated, their benefits and tradeoffs when applied to the circuit in fig. 2.3 compared, later on in chapter 4. Section 3.1 will describe the methodology used for selecting the size and bias points for transistors in the design while section 3.2 will define the selected circuit topology. Finally, section 3.3 gives a detailed description of the design process itself beginning with the initial parameter values obtained as a starting point and ending by providing the characterization, through simulations, of the two Op-Amps.

3.1 Design Methodology

Relevant to this thesis is the methodology proposed by Jespers and Murmann in [12] wherein the device's Transconductance Efficiency (g_m/I_D) is used as the main "knob" for selecting transistor parameters rather than the Overdrive Voltage (V_{OV}) approach found in most electronics textbooks [13], [14]. As explained in [12] the g_m/I_D of a transistor serves as a proxy for its inversion level and ranges from about 3 to 30 S/A for modern CMOS processes. This value is also linked to a number of width-independent metrics which will determine the device performance. Mainly, the direct relationship between g_m/I_D and Drain Current Density (I_D/W) allows for the sizing of devices based on the selected value of the bias Bias Drain Current (I_D), useful for this work due to the SR of Op-Amps being directly linked to the values of DC currents in the design [13].

The process for sizing and biasing the devices in this work was an approach combining hand-calculated values derived by applying analytical expressions to the specifications selected for the Op-Amp and simulations used to characterize the transistors. The calculated values set certain parameters and others are then selected based on data obtained from device simulations similar to the approach seen in [15].

The analytical expressions used in the initial hand analysis set constraints on each particular device in the design. These expressions will depend on the topology set for the Op-Amp and will be covered in detail under section 3.3.

As demonstrated in [15], a simulation is initially run for a single transistor, either NMOS or PMOS, sweeping its Gate-to-Source Voltage ($\mathrm{V_{GS}}$) from 0 to V_{DD} and channel length for a range of values of interest. The $\mathrm{V_{DS}}$ is kept at a constant value based on the DC point of operation set for the device from the Op-Amp topology. The quantities relevant to the constraints set on the device from the aforementioned hand-calculation analysis are then plotted against the $\mathrm{g_m/I_D}$. Furthermore, these parameters do not depend on the Total Gate Width (W) of the device allowing for the device to be sized based on the bias current and $\mathrm{I_D/W}$ [15].

The advantage of this method over traditional approaches is that the combination of actual simulation data with equations rather than a pure reliance on analytical models, allows for a more accurate prediction of how each device will behave individually in the final design. As a result the time spent tuning the design at the end of the process is greatly reduced. The designer can thus rely more on their knowledge of theory rather than needing to develop intuition through experience.

3.2 Design Topology

The approach throughout this project was to start by considering a simple design, moving on to more complex circuits if needed.

3.2.1 Amplifier Topology

Due to the required differential input range of 0.8 V_{PP} and a maximum closed loop gain of 2.85, the resulting output swing requirement for the Op-Amp is 2.28 V_{PP}. This means that each single-ended output of the amplifier must accommodate a swing of 1.14 V around its DC point. Therefore, a second stage to drive such an output range was deemed necessary. Furthermore, the nominal supply voltage of 0.8 V is insufficient to support such a voltage swing and will therefore have to be increased.

With these requirements in mind and considering the needed wide band and high speed operation of the Op-Amp, the design began with a simple two stage topology, depicted in figure 3.1 The first stage is an actively loaded differential pair while the second is a common source stage.

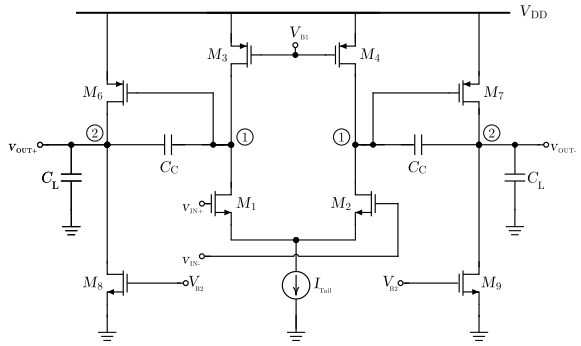


Figure 3.1: Schematic of a simple two stage Op-Amp without CMFB and biasing circuitry

3.2.2 Common Mode Feedback Topology

In fully differential Op-Amps the Common Mode (CM) level at the output is highly sensitive to device mismatches, which result in unpredictable biasing conditions for transistors in the circuit. Consequentially the output CM level is not well defined. For this reason, CMFB circuitry, which controls the biasing based on the detected CM variations at the output, thereby forcing a desired value, is necessary to ensure proper operation of the amplifier [13].

There exist several ways of realizing this CMFB circuitry. For the purposes of this thesis work a simple resistive sensing was chosen, keeping the resistance values high to ensure that they do not load the outputs [13].

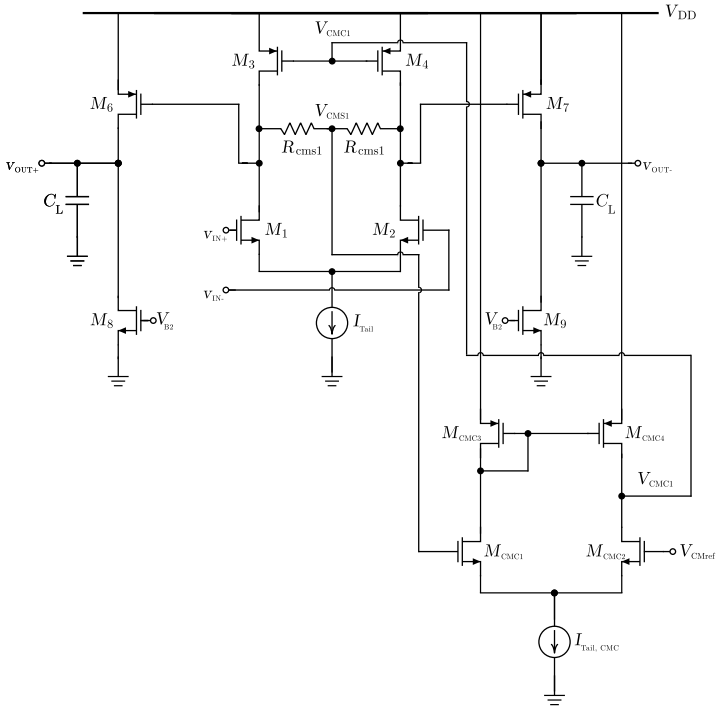


Figure 3.2: Schematic showing the CMFB applied to the first stage

The bias of the first stage is controlled by the use of an amplifier with its output connected to the gates of the PMOS load of the differential pair, seen in figure 3.2. Its inputs are connected to the first stage CM sensing node and a reference voltage, ensuring a stable value at the output of the first stage. If the voltage at the CM sensing node rises above the reference, the CMFB increases the bias at the PMOS gates, reducing their V_{GS}, thereby increasing the load resistance and lowering the output CM voltage. The opposite effect occurs if the CM output level falls below the reference [13].

For the second stage the NMOS loads have sensing resistors connected between the drain and gate terminals with a current source shown in figure 3.3 . The current source sets the bias V_{GS} for the load based on expression 3.1 [13].

$$V_{GS8,9} = V_{out,CM} - R_{cms2}\frac{I_Q}{2} \tag{3.1}$$

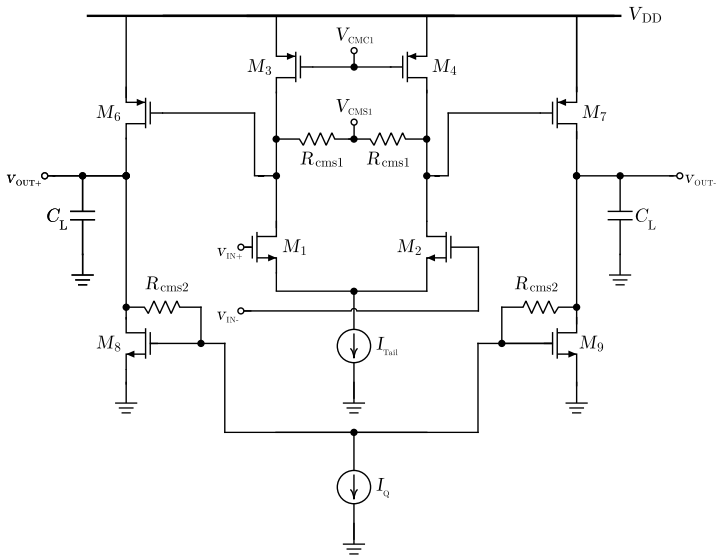


Figure 3.3: Schematic showing the CMFB of the second stage

3.2.3 Frequency Compensation for Two-stage Op-Amps

For any system connected in negative feedback to not oscillate the phase of its loop gain must be kept well above 180° at the frequency for which its magnitude reaches unity [13].

For Op-Amps this is crucial to ensure stable operation and as a consequence a performance metric know as Phase Margin (PM) is defined as the difference between the phase at unity loop gain and 180°. A value of 60° PM is typically considered optimal for stability and settling time and is therefore usually the target for Op-Amp designs [13].

The simple two-stage topology selected for the Op-Amp design in this thesis, shown in figure 3.1 may be seen as a two-pole system. The poles at nodes 1 and 2 (nodes are labeled the same for both sides since perfect symmetry is assumed) are closely spaced and defined by expressions 3.2 and 3.3 respectively [14]. With R_x and C_x being the total resistance and capacitance seen at node x ($x = 1, 2$).

$$p_1 = -\frac{1}{R_1 C_1} \tag{3.2}$$

$$p_2 = -\frac{1}{R_2 C_2} \tag{3.3}$$

Since each pole introduces a 90° phase shift to the amplifier frequency response, such closely spaced poles will usually result in a PM insufficient for stable operation.

As a result, it becomes necessary to compensate the frequency response of two-stage Op-Amps.

This compensation is typically done by introducing a capacitor connected between the outputs of the second and first stages as seen in figure 3.4, known as "Miller compensation". This method takes advantage of the high gain of the second stage, utilizing the miller effect to introduce a capacitance to node 1 resulting in an effect referred to as "pole splitting", depicted in figure 3.5 [13]. The poles, now found in expressions 3.4 and 3.5, are moved further apart with p_1 being moved toward the origin, becoming the dominant pole and the output pole p_2 being moved further away. This compensation however, also introduces a Right Half Plane (RHP) zero to the system due to the feedfoward path through C_C, given by expression 3.6.

$$p_1 = -\frac{1}{g_{m6,7} R_1 R_2 C_C} \tag{3.4}$$

$$p_2 = -\frac{g_{m6,7}}{C_1 + C_2} \tag{3.5}$$

$$z_1 = \frac{g_{m6,7}}{C_C} \tag{3.6}$$

A RHP zero will cause a phase shift in the frequency response, degrading the phase margin of the amplifier. There exist several techniques for removing this zero [16], two of which are relevant to this work and will be covered in detail further on in this section.

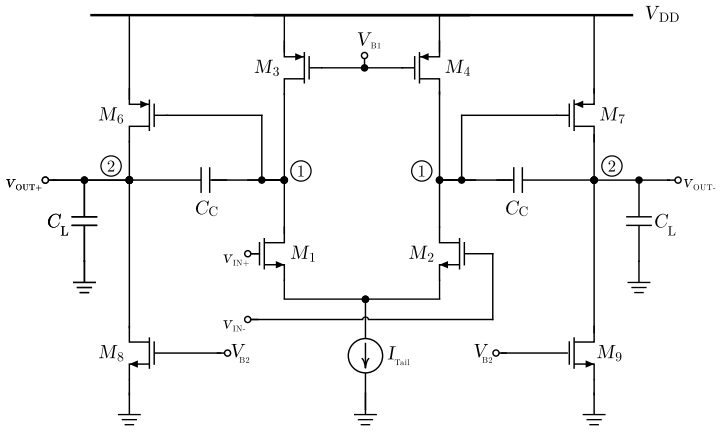


Figure 3.4: Schematic showing miller compensation for simple two-stage Op-Amp

Miller Compensation with Series RC Network

The most simple method for removing the RHP zero introduced in miller compensation consists of connecting a resistor (R_Z) in series with C_C, creating a series RC network. Figure 3.6 depicts this method applied to a fully differential Op-Amp. The zero is now given by expression 3.7 and is located in the Left Half Plane (LHP) if $R_Z > \frac{1}{g_{m6,7}}$.

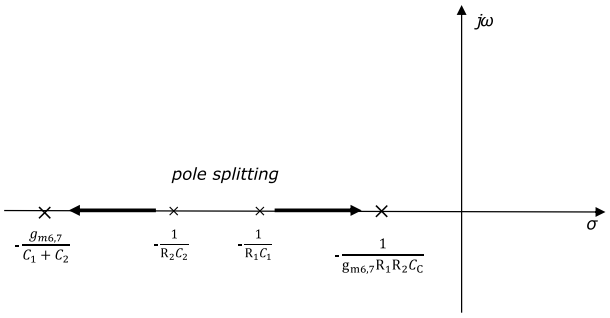


Figure 3.5: Pole splitting achieved by miller compensation

$$z_1 = \frac{1}{C_C(\frac{1}{g_{m6,7}} - R_Z)} \tag{3.7}$$

$$p_3 = -\frac{1}{C_1 R_Z} \tag{3.8}$$

In effect, the zero can now be pushed to infinity by setting $R_Z = \frac{1}{g_{m6,7}}$ or used to cancel the output pole (p_2) by setting $R_Z = \frac{C_1+C_L+C_C}{g_{m6,7}C_C}$. The resistor also introduces a third pole (expression 3.8) but it is usually located at very high frequencies for moderate values of R_Z [13].

This approach has the drawback that it is difficult to ensure a precise value for R_Z in actual implementation and the circuit may not behave predictably as a consequence [13].

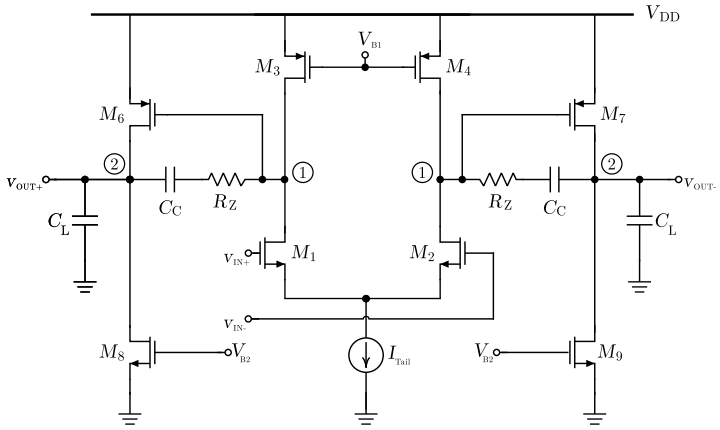


Figure 3.6: Schematic showing two-stage Op-Amp with series RC network miller compensation

Miller Compensation with Buffer

The zero introduced by miller compensation may be moved to the LHP by using a buffer to feedback the current flowing through C_C while avoiding the feedforward path caused by a direct connection [13], [17]. A simplified depiction of this method applied to a fully differential two-stage Op-Amp is depicted in figure 3.7. The approximate poles and zeroes found in this circuit are given by expressions 3.9-3.11 [13].

$$p_1 = -\frac{1}{g_{m1,2}R_1R_2C_C} \tag{3.9}$$

$$p_2 = -\frac{g_{m1,2}g_{m6,7}R_1}{C_2} \tag{3.10}$$

$$z_1 = -\frac{g_{m6,7}}{C_C} \tag{3.11}$$

The frequency of the non-dominant pole is now greater than in the previous method and the compensation does not load the first stage output, making this approach more suitable for wide band designs.

The main drawback for this method is that to ensure equal positive and negative slew rates the current flowing through the buffer must be at least as large as the tail current of the first stage, increasing the overall power consumption of the circuit [13].

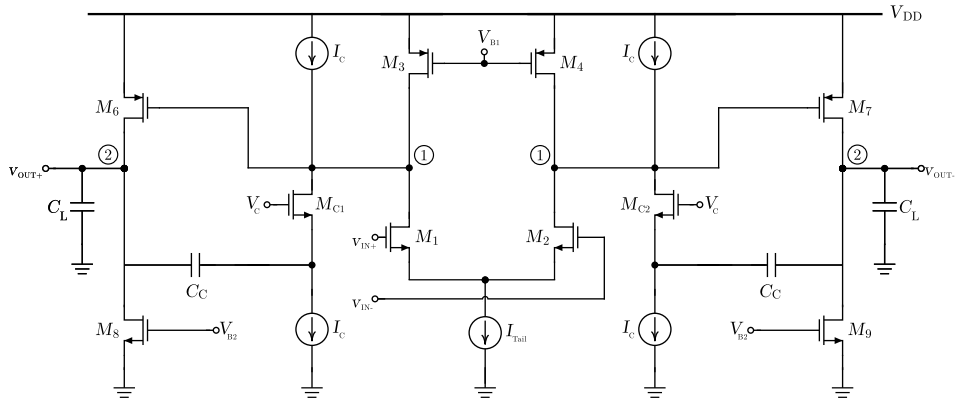


Figure 3.7: Simplified schematic showing two-stage Op-Amp with buffer for feeding current from C_C to the first stage

3.3 Design Process

With the underlying theory explained in the previous section, this section will serve to detail the process behind the Op-Amp designed for this work. The Op-Amp was designed to meet the specifications listed in table 2.2 and with the maximum closed loop gain configuration of 2.85 times in mind.

3.3.1 Determining Initial Parameter Values

Using the g_m/I_D based approach described in section 3.1, the initial values for the size and bias of each individual transistor were selected. Figure 3.8 shows the initial two-stage Op-Amp schematic. All devices were sized rounding the gate widths to integer multiples 1 μm.

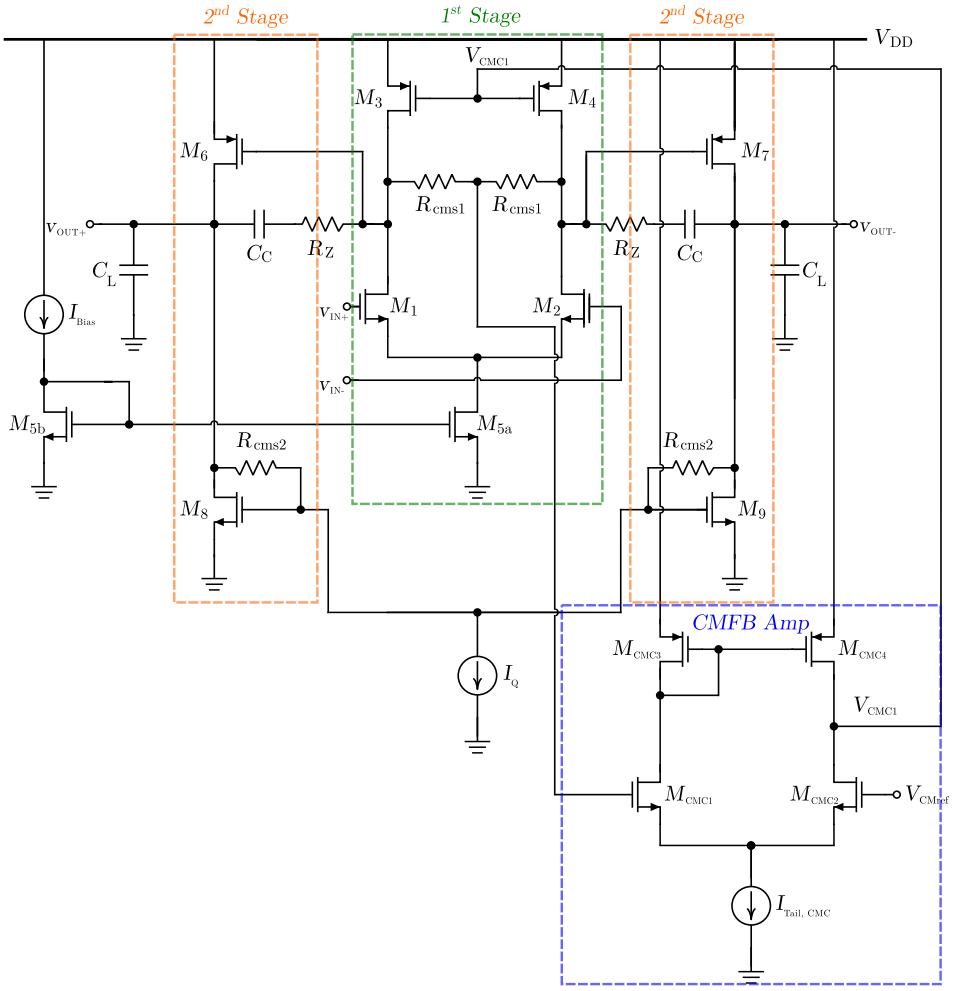


Figure 3.8: Initial Op-Amp design

Initial Calculations

Assuming that the non-dominant pole and miller RHP zero occur at much higher frequencies than the dominant pole ($f_{p_1} << f_{p_2}, f_{z_1}$), the PM of an Op-Amp may be approximated by eq. (3.12). Furthermore, assuming the load capacitance (C_L) to be greater than the capacitances seen at nodes 1 and 2 in fig. 3.8 (C_1 and C_2), the non-dominant

pole frequency can be found according to eq. (3.14) [18]. Here $g_{m1,2}$ and $g_{m6,7}$ are the respective Small Signal Transconductance (g_m) vales for M_{1-2} and M_{6-7} in fig. 3.8.

$$PM = 90^\circ - atan(\frac{GBW}{f_{p_2}}) - atan(\frac{GBW}{f_{z_1}}) \tag{3.12}$$

$$GBW = \frac{g_{m1,2}}{2\pi C_C} \tag{3.13}$$

$$f_{p_2} = \frac{g_{m6,7}}{2\pi(C_1 + C_2)} \approx \frac{g_{m6,7}}{2\pi C_L} \tag{3.14}$$

$$f_{z_1} = \frac{g_{m6,7}}{2\pi C_C} \tag{3.15}$$

Combining eqs. (3.13) to (3.15) results in eqs. (3.16) and (3.17) where $k = \frac{(g_m/I_D)_{1,2}}{(g_m/I_D)_{6,7}}$.

$$\frac{GBW}{f_{p_2}} = \frac{g_{m1,2}}{g_{m6,7}} \cdot \frac{C_L}{C_C} = k\frac{I_{D1,2}}{I_{D6,7}} \cdot \frac{C_L}{C_C} \tag{3.16}$$

$$\frac{GBW}{f_{z_1}} = \frac{g_{m1,2}}{g_{m6,7}} = k\frac{I_{D1,2}}{I_{D6,7}} \tag{3.17}$$

Now eq. (3.12) becomes eq. (3.18), allowing for a direct relation between C_L, C_C and the PM based on the selected ratios for the g_m/I_D of M_{1-2} and M_{6-7} and the DC bias currents of the first and second stages ($I_{D1,2}$ and $I_{D6,7}$).

$$PM = 90^\circ - atan(k\frac{I_{D1,2}}{I_{D6,7}} \cdot \frac{C_L}{C_C}) - atan(k\frac{I_{D1,2}}{I_{D6,7}}) \tag{3.18}$$

$$atan(x) + atan(y) = atan(\frac{x+y}{1-xy}) \quad , \quad xy < 1 \tag{3.19}$$

Applying the rule for the sum of inverse tangents given by eq. (3.19) (assuming $k^2(\frac{I_{D1,2}}{I_{D6,7}})^2(\frac{C_L}{C_C}) < 1$) and rearranging allows for the value of C_C to be determined based on eq. (3.20) from set values for k, C_L and the current ratio ($\frac{I_{D1,2}}{I_{D,6,7}}$).

$$C_C = \frac{k(\frac{I_{D1,2}}{I_{D,6,7}})(1 + tan(90^\circ - PM)k(\frac{I_{D1,2}}{I_{D,6,7}}))}{tan(90^\circ - PM) - k(\frac{I_{D1,2}}{I_{D,6,7}})} \cdot C_L \tag{3.20}$$

The SR of a two-stage Op-Amp is generally approximated with eq. (3.21). This assumes that the current of the first stage limits the SR, for this to hold $\frac{I_{D1,2}}{I_{D,6,7}}$ must satisfy eq. (3.22) [18].

$$SR = \frac{2I_{D1,2}}{C_C} \tag{3.21}$$

$$\frac{I_{D1,2}}{I_{D6,7}} \leqslant \frac{C_C}{2(C_L + C_C)} \tag{3.22}$$

Generally, a PM of *60°* is considered optimal for stability and settling time [13]. The initial value for C_C was calculated assuming the worst case $550\,fF$ C_L from table 2.2, with k and $\frac{I_{D1,2}}{I_{D,6,7}}$ set to *0.8* and *0.3* respectively, resulting in a C_C of *445 fF* from

eq. (3.20). Applying this to eq. (3.21) gives a minimum total current of *3.83 mA* for the first stage. This was rounded up to *4 mA* for the design, thereby setting $I_{D1,2}$ to *2 mA*. With the selected current ratio of *0.3*, $I_{D6,7}$ now evaluates to *6.67 mA*. It can be proven that these parameters satisfy eq. (3.22).

The $\mathrm{g_m/I_D}$ values are determined to be *10 S/A* and *12.5 S/A* for the input transistors of the first and second stage respectively from eqs. (3.23) and (3.24) (eq. (3.23) is derived by combining eqs. (3.13) and (3.21)).

$$(\frac{g_m}{I_D})_{1,2} = \frac{4\pi GBW}{SR} \tag{3.23}$$

$$(\frac{g_m}{I_D})_{6,7} = k^{-1}(\frac{g_m}{I_D})_{1,2} \tag{3.24}$$

To ensure that all devices operate in the active region eqs. (3.25) to (3.28) must be satisfied according to the input and output voltage swings specified in table 2.2.

$$v_{IN,min} \geqslant V_{DS5} + V_{th1,2} \tag{3.25}$$

$$v_{IN,max} \leqslant V_{DD} - |V_{Dsat3,4}| \tag{3.26}$$

$$v_{OUT,min} \geqslant V_{Dsat8,9} \tag{3.27}$$

$$v_{OUT,max} \leqslant V_{DD} - |V_{Dsat6,7}| \tag{3.28}$$

The input voltage range from $v_{IN,min} = V_{DS5} + V_{GS1,2} - 0.2\,V$ to $v_{IN,max} = V_{DS5} + V_{GS1,2} + 0.2\,V$ for a single ended swing of $0.4\,V_{PP}$, combined with eqs. (3.25) and (3.26) results in the constraints on the first stage set by eqs. (3.29) and (3.30).

$$V_{GS1,2} \geqslant V_{th1,2} + 0,2\,V \tag{3.29}$$

$$|V_{Dsat3,4}| \leqslant V_{DD} - (V_{DS5} + V_{GS1,2} + 0.2\,V) \tag{3.30}$$

For the second stage, the output voltage range in the maximum gain configuration, which becomes $v_{OUT,min} = V_{OUT,CM} - 0.57\,V$ and $v_{OUT,max} = V_{OUT,CM} + 0.57\,V$ for a 1.14 V_{PP} single ended output swing, sets the constraints given by eqs. (3.31) and (3.32).

$$V_{Dsat8,9} \leqslant V_{OUT,CM} - 0.57\,V \tag{3.31}$$

$$|V_{Dsat6,7}| \leqslant V_{DD} - (V_{OUT,CM} + 0.57\,V) \tag{3.32}$$

Selecting the common mode output voltage for the second stage as $V_{OUT,CM} = V_{DD}/2$ to maximize output swing, yields a maximum V_{Dsat} of $0.23\,V$ for M_{6-9}.

Table 3.1 shows all the parameter values and constraints obtained through initial hand calculations.

Parameter	Value
C_L	550 fF
C_C	445 fF
$I_{D1,2}$	2 mA
$I_{D6,7}$	6.67 mA
$(g_m/I_D)_{1,2}$	10 S/A
$(g_m/I_D)_{6,7}$	12.5 S/A
$V_{GS1,2}$	$\geqslant V_{th1,2} + 0,2\,V$
$\lvert V_{Dsat3,4}\rvert$	$\leqslant V_{DD} - (V_{DS5} + V_{GS1,2} + 0.2\,V)$
$\lvert V_{OUT,CM}\rvert$	$0.8\,V$
$\lvert V_{Dsat6,7}\rvert$	$\leqslant 0.23\,V$
$V_{Dsat8,9}$	$\leqslant 0.23\,V$

Table 3.1: Table showing parameter values and constraints obtained from initial hand calculations for Op-Amp design

First Stage Design

With a $1.6\,V$ supply the DC bias point $\mathrm{V_{DS}}$ were selected as $0.5\,V$, $0.55\,V$ and $0.55\,V$ for M_{3-4}, M_{1-2} and M_5 respectively to set a $0.5\,V$ $\mathrm{V_{GS}}$ for M_{6-7} in the second stage. Keeping a high $\mathrm{V_{GS}}$ on M_{6-7} will allow for higher $\mathrm{g_m}$ values to be achieved with a smaller size, resulting in reduced overall parasitic capacitances of these devices and lower values of C_1 and C_2. This is done to ensure wide spacing between the dominant (p_1) and non-dominant (p_2) poles by pushing p_2 to a high frequency (eq. (3.5)).

The Channel Length (L) values for M_{1-4} were set to the minimum allowed $20\,nm$ by the Process Design Kit (PDK) to minimize the total capacitance seen at the output of the first stage. L for M_5 was set to $100\,nm$ in order to achieve a high output resistance as this device acts as a current source for the first stage.

As explained in section 3.1, with a predetermined value for the $\mathrm{V_{DS}}$ and L, all other relevant, W independent parameters are plotted against the $\mathrm{g_m/I_D}$ of the device based on results obtained from a DC analysis $\mathrm{V_{GS}}$ sweep. Relevant parameters plotted against $\mathrm{g_m/I_D}$ for NMOS and PMOS at channel lengths of interest are shown in figs. 3.9 and 3.10 (W set to $1\,\mu m$ in analysis).

Considering the constraint set on $V_{GS1,2}$ set by table 3.1 and observing fig. 3.9a it may be concluded that the maximum allowable $\mathrm{g_m/I_D}$ for M_{1-2} is $8.83\,S/A$, resulting in a conflict with the initial calculated value of $10\,S/A$. Rather than re-doing all the initial calculations it was decided to set $(g_m/I_D)_{1,2}$ to $8.5\,S/A$ (leaving some headroom) and move on with the design. This is justified by the fact that the initial value for $(g_m/I_D)_{1,2}$ is found from eq. (3.23) based on the required $\mathrm{g_m}$ and $\mathrm{I_D}$ to meet the GBW and SR specifications for the Op-Amp. Simply scaling the widths of all devices in the first stage allows for a proportional increase in the $\mathrm{I_D}$ of the first stage while keeping all other metrics the same [13], increasing the SR according to eq. (3.21), thereby reducing the required value for $(g_m/I_D)_{1,2}$ (the second stage would then also have to be scaled by the same amount to keep the $\mathrm{I_D}$ ratio).

With the selected $(g_m/I_D)_{1,2}$, all other relevant quantities for M_{1-2} may be read

from figs. 3.9b and 3.9c. $V_{GS1,2}$ is set to $0.43\,V$ and by applying eq. (3.33) $W_{1,2}$ is found to be $10.23\,\mu m$, which is rounded down to $10\,\mu m$.

$$W = \frac{I_D}{(I_D/W)} \tag{3.33}$$

The bias current for the first stage is supplied by M_{5a} which mirrors an external DC current as depicted in fig. 3.8. For a current mirror to operate properly the $\mathrm{V_{DS}}$ of the devices must be equal [13]. Since the current source for the first stage is designed as a 1:1 current mirror, the constraint $V_{DS5a} = V_{DS5b}$ is set. M_{5b} is diode connected, hence $V_{DS5b} = V_{GS5b}$ and as a consequence $V_{DS5a} = V_{GS5b} = V_{GS5a}$. Now the $\mathrm{g_m/I_D}$ value for which $V_{GS5a} = V_{DS5a} = 0.55\,V$ is found to be $8.7\,S/A$ in fig. 3.9b ($L_{5a} = 100\,nm$). Applying eq. (3.33) to $(I_D/W)_{5a}$ read from fig. 3.9c gives $W_{5a} = 39.67\,\mu m$, rounded up to $40\,\mu m$ for the design.

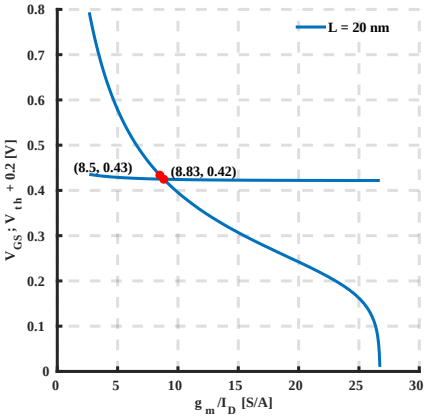
According to the values determined for $V_{GS1,2}$ and V_{DS5} the constraint on $|V_{Dsat3,4}|$ becomes $|V_{Dsast3,4}|_{max} = 0.42\,V$ which is satisfied by any value for $(g_m/I_D)_{3,4}$ when looking at fig. 3.10b. In essence, the design for M_{3-4} is unconstrained and therefore an arbitrary initial $(g_m/I_D)_{3,4}$ of $8.5\,S/A$ was chosen to match the value for M_{1-2}. Inserting the value read from fig. 3.10c into eq. (3.33) results in $W_{3,4} = 17.079\,\mu m$, rounded to $17\,\mu m$. $V_{GS3,4}$ is found to be $0.47\,V$ from fig. 3.10a, this sets the required DC output voltage for the CMFB amplifier explained in section 3.2.2.

$$V_{CM,IN} = V_{GS1,2} + V_{DS5a} \tag{3.34}$$

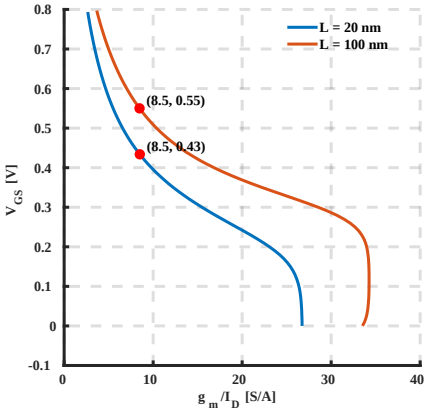
Table 3.2 summarizes the initial values obtained for the first stage. The CM input voltage is selected based on eq. (3.34) and is found to be $0.98\,V$, rounded up to $1\,V$ for simulations later.

Parameter	$\boldsymbol{M_{1-2}}$	$\boldsymbol{M_{3-4}}$	$\boldsymbol{M_{5a,b}}$
$V_{DS}\ [V]$	0.55	0.5	0.55
$L\ [nm]$	20	20	100
$W\ [\mu m]$	10	17	40
$V_{GS}\ [V]$	0.43	0.47	0.55
$I_D\ [mA]$	2	2	4

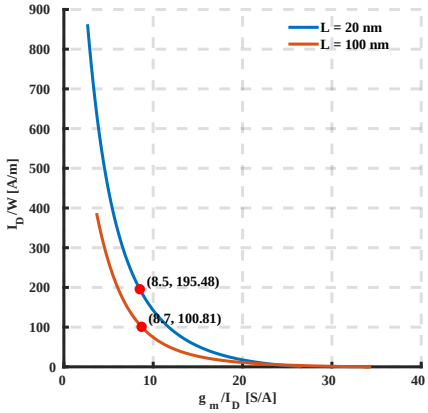
Table 3.2: Table showing parameter values and constraints obtained from initial hand calculations for Op-Amp design



(a) Plot showing NMOS V_{GS} and $V_{th} + 0.2\,V$ against g_m/I_D, $V_{DS} = 0.55\,V$

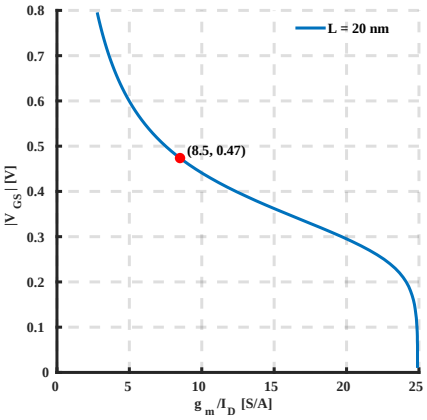


(b) Plot showing NMOS V_{GS} against g_m/I_D, $V_{DS} = 0.55\,V$

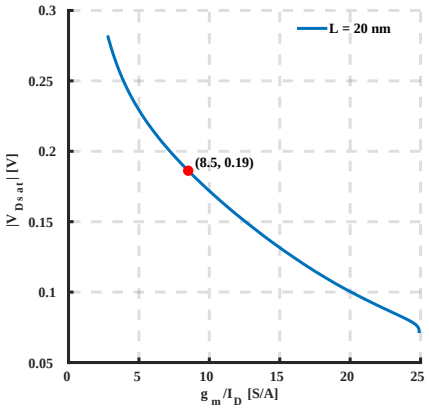


(c) Plot showing NMOS I_D/W against g_m/I_D, $V_{DS} = 0.55\,V$

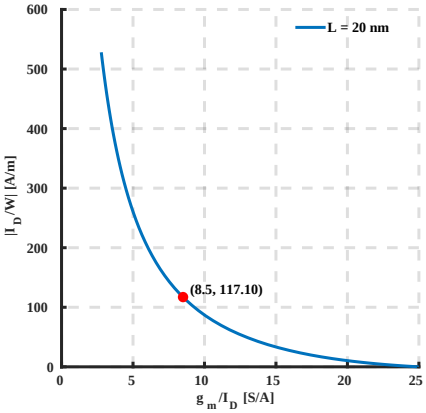
Figure 3.9: NMOS characteristics plotted against g_m/I_D for M_{1-2} $(L_{1,2} = 20\,nm)$ and $M_{5a,b}$ $(L_5 = 100\,nm)$



(a) Plot showing PMOS V_{GS} against $g_m/I_D, V_{DS} = 0.5\,V$



(b) Plot showing PMOS V_{Dsat} against $g_m/I_D, V_{DS} = 0.5\,V$



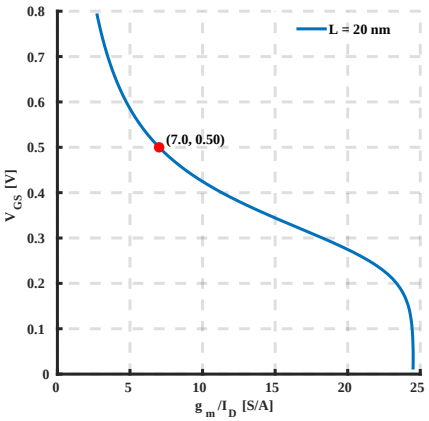
(c) Plot showing PMOS I_D/W against $g_m/I_D, V_{DS} = 0.5\,V$

Figure 3.10: PMOS characteristics plotted against g_m/I_D for M_{3-4} $(L_{3,4} = 20\,nm)$

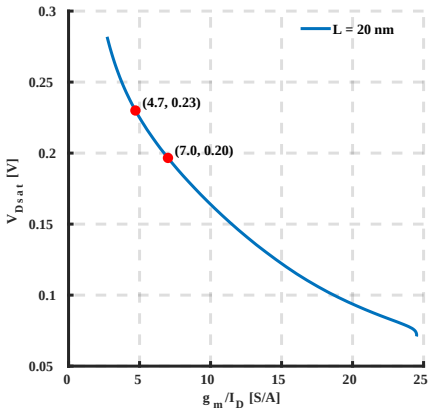
Second Stage Design

The common mode output voltage from table 3.1 sets the V_{DS} values for the devices in the second stage. Figures 3.11 and 3.12 depict all relevant parameters plotted against g_m/I_D for V_{DS} set to $0.8\,V$.

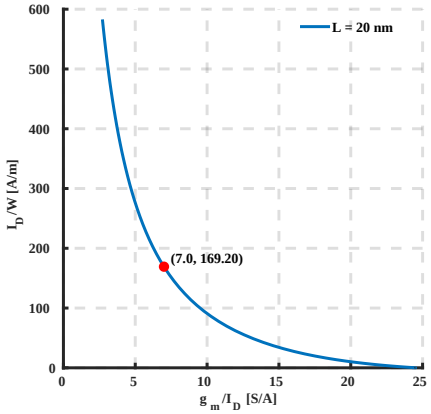
The main constraint on M_{6-7} is set by the V_{DS} of M_{3-4} from the previous stage. Figure 3.11a shows that for $V_{GS6,7} = V_{DS6,7} = 0.5\,V$ the g_m/I_D for M_{6-7} is $7\,S/A$. This value is above the minimum required g_m/I_D observed in fig. 3.11b based on the $|V_{Dsat6,7}|$ constraint from table 3.1. Applying the value read from fig. 3.11c to eq. (3.33) results in $W_{3,4} = 39.421\,\mu m$, rounded to $40\,\mu m$.



(a) Plot showing PMOS V_{GS} against $g_m/I_D, V_{DS} = 0.8\,V$



(b) Plot showing PMOS V_{Dsat} against $g_m/I_D, V_{DS} = 0.8\,V$

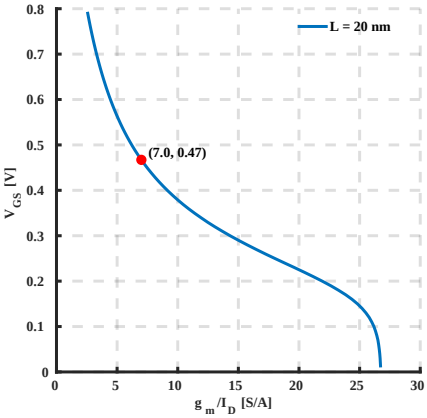


(c) Plot showing PMOS I_D/W against $g_m/I_D, V_{DS} = 0.8\,V$

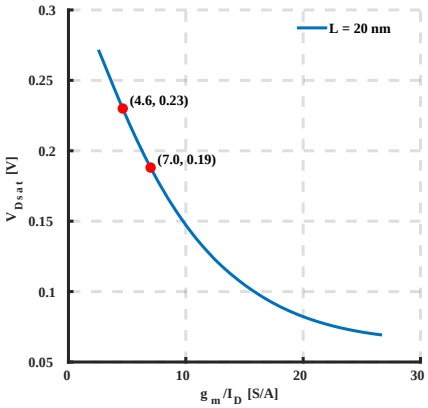
Figure 3.11: PMOS characteristics plotted against g_m/I_D for M_{6-7} $(L_{6,7} = 20\,nm)$

The only constraint on M_{8-9} applies to the maximum value for $V_{Dsat8,9}$ found in table 3.1. Figure 3.12b sets the minimum g_m/I_D for M_{8-9} to $4.6\,S/A$. To leave some

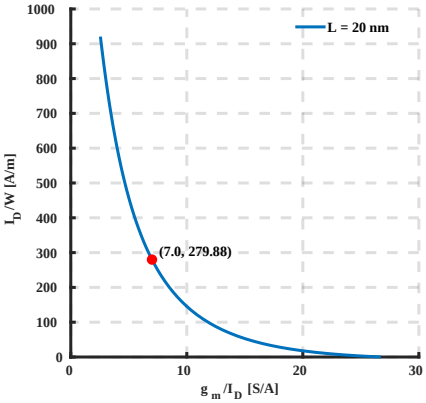
V_{Dsat} headroom the g_m/I_D was set to an arbitrary initial value of $7\,S/A$ (matching $(g_m/I_D)_{6,7}$). From fig. 3.12c and eq. (3.33) $W_{8,9} = 23.832\,\mu m$ is obtained, rounded to $24\,\mu m$. $V_{GS8,9}$ is found as $0.47\,V$ from fig. 3.12a.



(a) Plot showing NMOS V_{GS} against $g_m/I_D, V_{DS} = 0.8\,V$



(b) Plot showing NMOS V_{Dsat} against $g_m/I_D, V_{DS} = 0.8\,V$



(c) Plot showing NMOS I_D/W against $g_m/I_D, V_{DS} = 0.8\,V$

Figure 3.12: NMOS characteristics plotted against g_m/I_D for M_{8-9} $(L_{8,9} = 20\,nm)$

Table 3.3 gives a summary of all the initial parameter values obtained for the second stage.

Parameter	M_{6-7}	M_{8-9}
$V_{DS}\ [V]$	0.8	0.8
$L\ [nm]$	20	20
$W\ [\mu m]$	40	24
$V_{GS}\ [V]$	0.5	0.47
$I_D\ [mA]$	6.67	6.67

Table 3.3: Table showing parameter values and constraints obtained from initial hand calculations for Op-Amp design

Frequency Compensation

The initial value for the resistor in the RC frequency compensation seen in fig. 3.8 was chosen according to eq. (3.35), where the sum of C_1 and the parasitic capacitance component of C_2 was assumed to be a total of $150\,fF$. As a result, the initial value for R_Z evaluates to $53.526\,\Omega$ ($g_{m6,7} = (g_m/I_D)_{6,7} \cdot I_{D6,7}$).

$$R_Z = \frac{C_1 + C_2 + C_C}{g_{m6,7}C_C} \approx \frac{C_L + C_C + 150\,fF}{g_{m6,7}C_C} \tag{3.35}$$

The Op-Amp was at first evaluated only with miller RC frequency compensation and the buffer method was introduced at a later point. Hence, this was not considered during the initial design step and will be covered later in section 3.3.

First Stage Common Mode Feedback

To sense the output CM level for the first stage a simple resistive sensing was implemented seen as R_{cms1} in fig. 3.8. The values for these resistors were set to $100\,k\Omega$ each to prevent resistive loading at the first stage output by ensuring $R_{cms1} >> R_1 = (r_{out1,2}||r_{out3,4})$.

For the first stage CMFB, as explained in section 3.2.2, an amplifier comparing the difference between the sensed CM output of the first stage at node CMS in fig. 3.8 and a reference voltage was connected to the gates of the PMOS load (M_{3-4}) to force a desired value at the first stage output. Since there were no real requirements set on this amplifier it was deemed acceptable to start with a simple 5 transistor amplifier shown in fig. 3.2, setting all devices to the minimum unit size of $(W/L) = \frac{1\,\mu m}{20\,nm}$ used in this project and the bias current ($I_{Tail,CMC}$) to $50\,\mu A$, altering these values if problems were encountered later during simulations.

Second Stage Common Mode Feedback

The CMFB for the second stage was explained in section 3.2.2. Now, reordering eq. (3.1) gives eq. (3.36). Applying the known values for $V_{GS7,8}$ and $V_{OUT,CM}$ while setting R_{cms2} to $100\,k\Omega$ to prevent resistive loading at the output, yields $I_Q = 6.6\,\mu A$.

$$I_Q = 2 \cdot \frac{(V_{OUT,CM} - V_{GS8,9})}{R_{cms2}} \tag{3.36}$$

Figure 3.13 shows the complete initial Op-Amp design with all parameter values annotated.

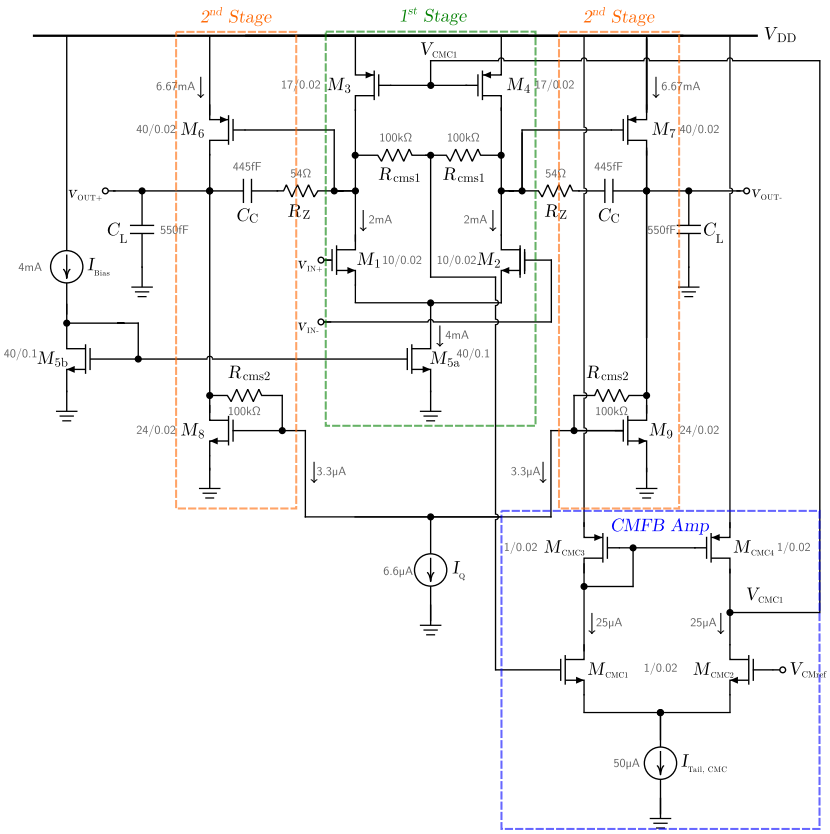


Figure 3.13: Initial Op-Amp design with annotations for all parameter values

3.3.2 Initial Design Simulation and Tuning

Figure 3.14 shows the Closed-Loop (CL) AC differential gain magnitude plotted against frequency for the initial design in the maximum gain configuration. As can be seen, the GBW for the initial design is significantly lower than the specified $6.84\,GHz$ from table 2.2 which was originally estimated. This is likely due to the reduction of $(g_m/I_D)_{1,2}$ explained in section 3.3.1. Also, observing the DC bias point of the first stage after simulation showed a mismatch between the selected values for $\mathrm{V_{DS}}$ on M_{1-2} and M_5 ($\mathrm{V_{DS}}$ for M_{3-4} is forced to $0.5\,V$ by the CMFB), suggesting the need to resize these devices.

The parameter values were therefore tuned to achieve improved results. The methodology used in this thesis having the advantage of reducing the overall time spent on tuning by having a robust staring point and as will later be seen, the values in the final design do

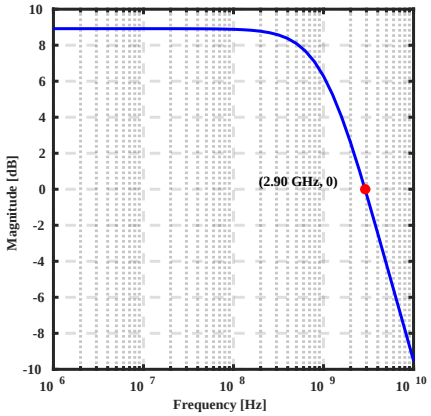


Figure 3.14: Initial Op-Amp closed-loop magnitude response in maximum gain configuration

not deviate significantly from those obtained in section 3.3.1. The final tuned Op-Amp design with all parameter values annotated is depicted in fig. 3.15 (tuned values highlighted in red).

Firstly, the load requirement was reduced to the minimal $100\,fF$ from table 2.2, to simplify the design process. This relaxation of the requirement on the capacitive load which the Op-Amp must drive was deemed acceptable since a buffer may always be introduced after the amplifier to mitigate the loading it experiences from the subsequent circuitry. Furthermore, this allowed for the reduction of the compensation capacitance (now $C_C = 120\,fF$) and combined with resizing the first stage (M_{1-5}) resulted in a significant increase to the GBW while maintaining a stable 59.1° PM in unity gain configuration (worst-case scenario for PM [13]) as depicted in fig. 3.16a.

The new results for CL AC differential gain magnitude in maximum gain configuration can be seen in fig. 3.16b demonstrating a significant improvement to the GBW achieved by the Op-Amp.

Observing the phase characteristic of the Op-Amp in fig. 3.16b, the main limitation of the design may be noted. Namely, the frequency starts to shift way before the intended $2.4\,GHz$ BW required for the APD system to handle the worst case $1.6\,GHz$ signal explained in chapter 2, ending up at -25.2°.

Further tuning of the design proved ineffective. Extending the phase shift to higher frequencies resulted in the amplifier becoming unstable (insufficient PM in unity gain configuration). After extended testing the RC compensation was deemed to be the main limiting factor for the design and therefore an alternative compensation approach will be explored later in section 3.3.3.

The slewing behavior for the Op-Amp is depicted in fig. 3.17 as the step response of the amplifier for a rail-to-rail input step. In fig. 3.17a the falling SR is found to be $21.56\,V/ns$ as the 90% to 10% fall time for the output whereas the rising SR is measured as $18.385\,V/ns$ in fig. 3.17b as the 10% to 90% rise time. These measured values exceed the original $8.6\,V/ns$ requirement for the design due to the reduction of both C_L and C_C.

In fig. 3.18 the Op-Amp response to a $2.4\,GHz$ and differential $0.8\,V_{PP}$ sinusoid in maximum gain configuration from transient analysis is depicted. As expected, there is no

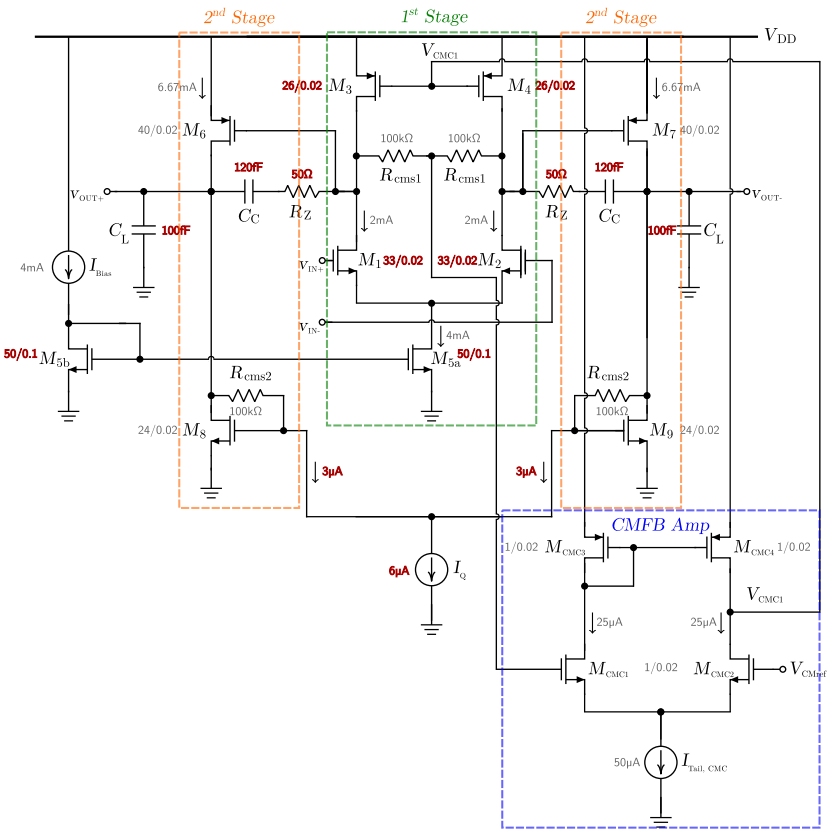
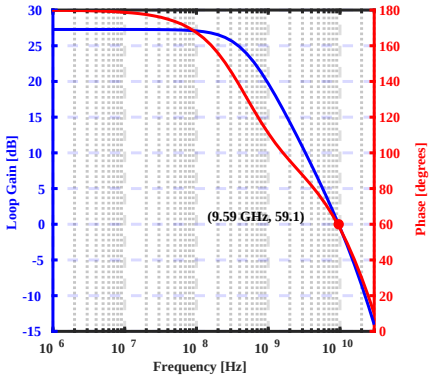
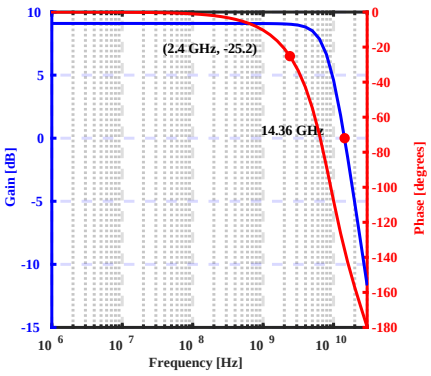


Figure 3.15: Final RC compensated Op-Amp design schematic with annotations for all parameter values

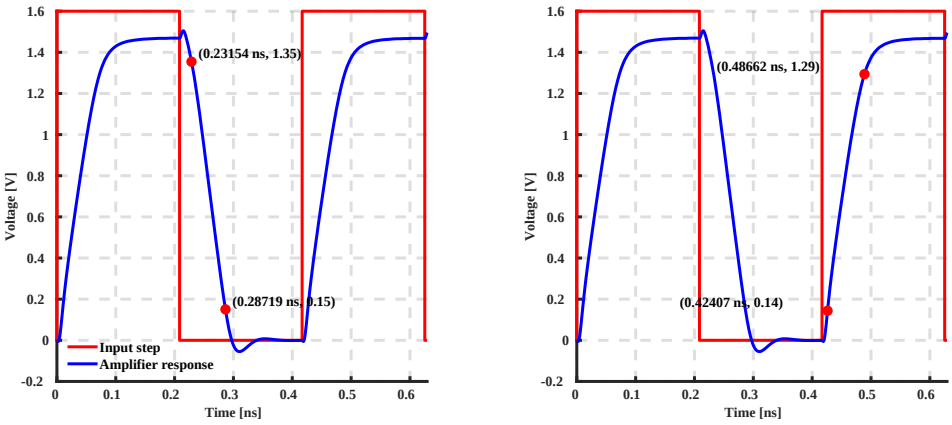


(a) Loop gain frequency response in unity gain configuration



(b) Closed-loop frequency response in maximum gain configuration

Figure 3.16: Tuned Op-Amp frequency response



(a) Op-Amp step response showing points for falling SR calculation

(b) Op-Amp step response showing points for rising SR calculation

Figure 3.17: Step response of RC miller compensated Op-Amp

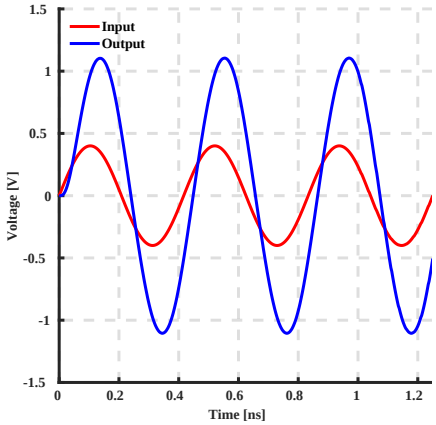


Figure 3.18: Transient input and output waveforms at $2.4\,GHz$ frequency for RC compensated Op-Amp in maximum gain configuration

Amplitude-to-Amplitude (AM-AM) distortion in the waveforms but the phase shift seen at $2.4\,GHz$ in fig. 3.16b is confirmed by the delay present between the input and output.

3.3.3 Indirect Frequency Compensated Op-Amp Simulations

Indirect miller compensation, explained in section 3.2.3, removes the need for a zero-nulling resistor and allows for a reduced value of C_C (now $70\,fF$), extending the BW [17]. As described in [17], a buffer is introduced to the design to remove the feedforward path formed by directly connecting C_C between the outputs of the two stages. The buffer was implemented using a common gate device biased to drive a current equal in value

to that of the total in first stage ($4\,mA$). Due to the design being fully differential two such buffers were implemented on each side. The biasing for the common gate device in the buffer was implemented as in [19] to force equal currents flowing through $M_{C1,2up}$ and $M_{C1,2down}$. Furthermore, the best performance was observed when setting the DC voltage at the buffer gate terminal to $1.2\,V$. Figure 3.19 depicts the schematic for the indirectly compensated Op-Amp with all parameter values annotated.

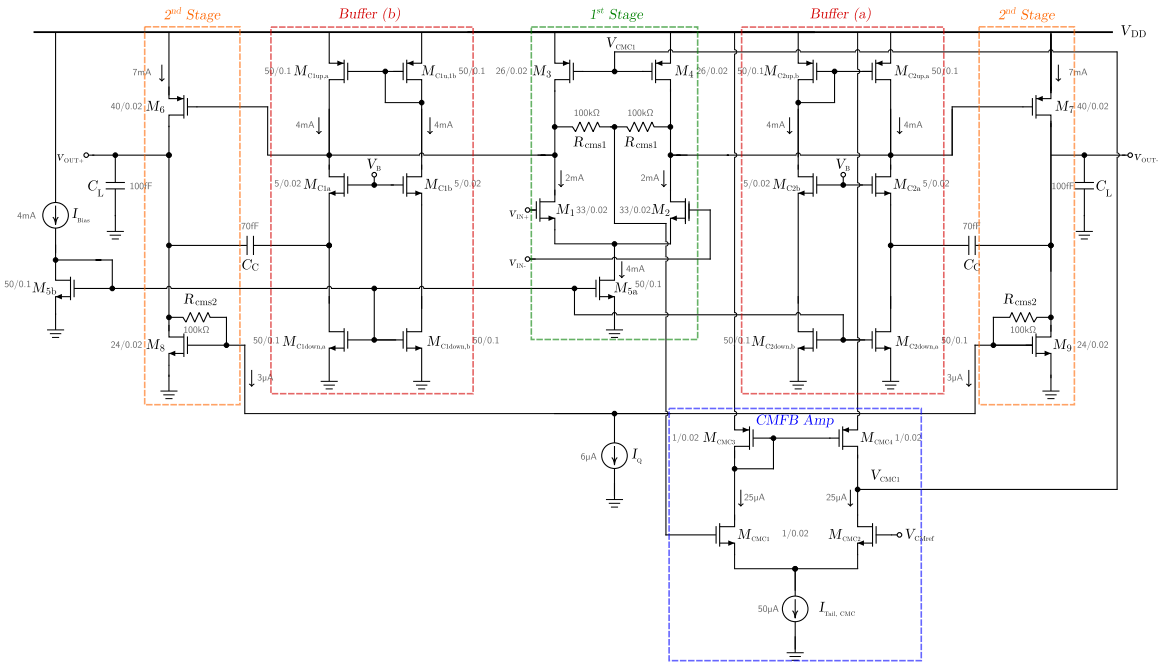


Figure 3.19: Indirectly compensated Op-Amp design schematic with annotations for all parameter values

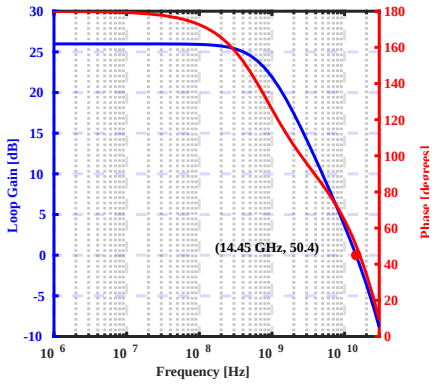
Figure 3.20a shows the loop gain and phase in unity gain configuration for the indirectly compensated Op-Amp, demonstrating a stable $50.4°$ PM.

In fig. 3.20b the AC gain magnitude and phase characteristics are depicted. The GBW is now significantly higher at $20.89\,GHz$ and the phase shift at $2.4\,GHz$ has been reduced by $8.1°$.

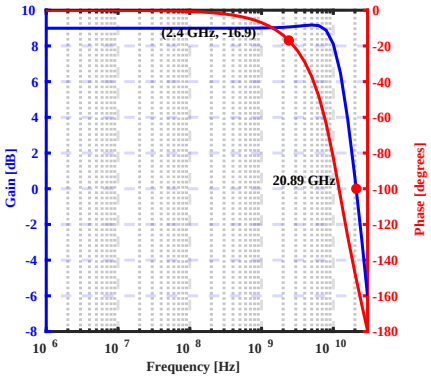
Figures 3.21a and 3.21b depict the slewing behavior of the indirectly compensated Op-Amp. The falling and rising SR are found to be $38.28\,V/ns$ and $28.06\,V/ns$ respectively from these plots showing a significant improvement over the RC compensated design.

Comparing the transient responses in figs. 3.18 and 3.22 the reduction in phase shift at $2.4\,GHz$ is confirmed.

Overall the indirect compensation demonstrates a significantly improved BW and SR at the cost of increased current consumption. The current consumed by the design may be obtained as the sum of all currents annotated for the branches in fig. 3.19 (also accounting for the $50\,\mu A$ in the CMFB), giving a total value of $34.05\,mA$, a significant increase when compared to the total $17.39\,mA$ consumed by the RC compensated design in fig. 3.15.

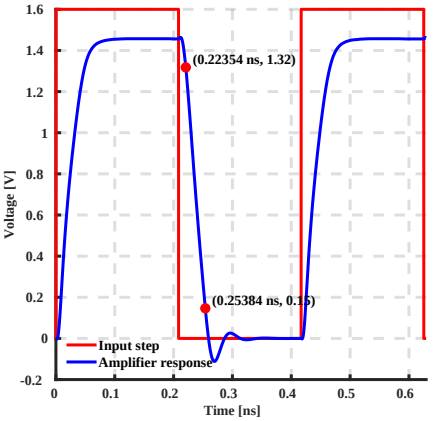


(a) Loop gain frequency response in unity gain configuration

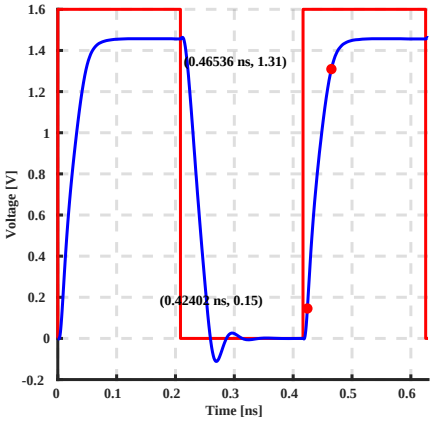


(b) Closed-loop frequency response in maximum gain configuration

Figure 3.20: Indirect miller compensated Op-Amp frequency response



(a) Op-Amp step response showing points for falling SR calculation



(b) Op-Amp step response showing points for rising SR calculation

Figure 3.21: Step response of indirect miller compensated Op-Amp

A key fact which must be considered at this point is that the current consumed in the indirectly compensated design may be significantly reduced by optimizing the bias network. Due to time constraints, more effective biasing was not explored during this project but through proper configuration of the current mirrors used to bias the compensation buffer it would be possible to achieve a great reduction in the total current. As an example configuring the current mirrors to 1:50 instead of 1:1 would result in a total of $26.21\,mA$. This optimization is left to future work and the current consumed by the Op-Amp will henceforth be considered disregarding the bias network, ending up at $26.05\,mA$.

The two designs depicted in figs. 3.15 and 3.19 will be further compared with the intended FB network applied in chapter 4. Table 3.4 provides an overview of the performance metrics of the two Op-Amps designed in this chapter.

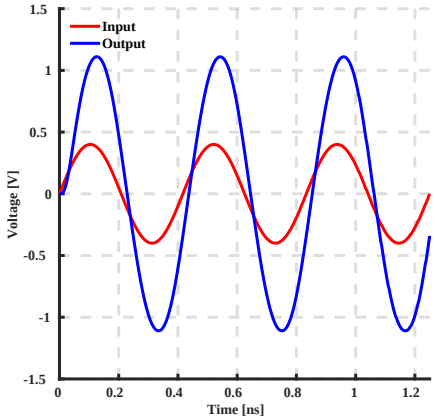


Figure 3.22: Transient input and output waveforms at $2.4\,GHz$ frequency for indirect miller compensated Op-Amp in maximum gain configuration

Op-Amp Performance Metric	**RC compensated**	**Indirectly compensated**
GBW in maximum gain [GHz]	14.36	20.89
PM in unity gain [$^\circ$]	59.1	50.4
Phase at $2.4\,GHz$ *[$^\circ$]*	-25.2	-16.9
SR_{min} *[V/ns]*	18.385	28.06
Total DC current [mA] (without bias)	17.39	26.05
$P_{DC}\,[mW]$ *(without bias)*	27.824	41.68

Table 3.4: Table showing parameter values and constraints obtained from initial hand calculations for Op-Amp design

Chapter 4

Feedback Network Design and System Performance Evaluation

This chapter will cover the design and implementation of the FB network applied to the Op-Amp designed in chapter 3 to realize the gain expansion function defined in chapter 2. It is divided into two main sections. Section 4.1 covers the design of the switched resistive FB achieving the desired switching behavior as well as the gain values specified in table 2.1 and section 4.2 discusses the current injection scheme implemented as a way of smoothing out the transitions, ensuring a piecewise linear transfer characteristic for the circuit.

4.1 Switched Resistive Feedback Network Design and Simulation Results

4.1.1 Conceptual Background

FB is a technique which finds wide-spread application in analog circuits. When designing amplifiers, a form known as negative FB is applied, the benefits of which include gain desensitization, non-linearity reduction and increased BW among others [13]. Several different variations of FB exist and may be selected depending on the intended functionality and performance of the circuit.

For the work in this project, a switched resistive negative FB, depicted in fig. 2.3, is proposed as a way to dynamically alter the circuit gain during operation. From this point on the term FB refers to negative FB specifically.

Resistive Feedback

Resistive FB, wherein a ratio of resistors defines the gain, is typically applied to amplifiers with the intention of achieving a stable and predictable output characteristic. Figure 4.1 illustrates a basic example of such a FB applied to a fully differential Op-Amp. The overall differential gain of the circuit is found in eq. (4.1) where $\beta = \frac{R_s}{R_f}$ is the feedback factor and A is the Open-Loop (OL) gain of the amplifier.

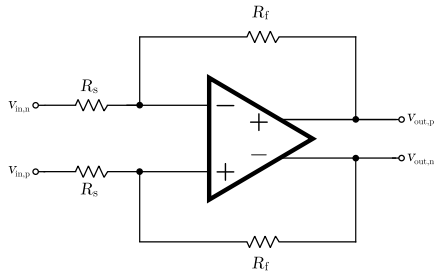


Figure 4.1: Example of resistive negative feedback applied to a fully differential Op-Amp

$$A_{Vtot,DM} = \frac{v_{OUT+} - v_{OUT-}}{v_{IN+} - v_{IN-}} = \frac{A}{1+\beta A} = \frac{1}{\beta}(1 - \frac{1}{1+\beta A}) \approx \frac{1}{\beta}(1 - \frac{1}{\beta A}) \quad (4.1)$$

The term βA in eq. (4.1) is known as the loop gain of the circuit and the approximation seen in this expression is valid for a high value of this quantity ($\beta A >> 1$). For amplification β must be less than unity and therefore a large loop gain is achieved if the OL gain of the amplifier (A) is high. When this condition is met the differential gain simplifies to eq. (4.2).

$$A_{Vtot,DM} = \frac{v_{OUT+} - v_{OUT-}}{v_{IN+} - v_{IN-}} \approx \frac{1}{\beta} = \frac{R_f}{R_s} \quad (4.2)$$

Since the OL gain of Op-Amps is typically a large value this allows for the circuit gain to be determined by a ratio of resistors instead of the amplifier itself, making it much more well defined during operation [13].

Switched Resistive Feedback

The main intention behind applying a switched resistive FB to the Op-Amp in this work is to enable the circuit gain to be controlled dynamically during operation.

The concept is best understood by observing fig. 4.2, the resistor branches (5 in total for each end) are connected in parallel and each branch, with the exception of the innermost one, consists of a switch in series with a resistor. Depending on the states of each switch, the overall resistance in the feedback is determined as a parallel connection of the branches for which the switches are closed.

An external system controls the switches by detecting when the input signal reaches the threshold values set in table 2.1. These values determine the breakpoints for the transfer function.

Initially all switches are closed and the lowest gain value (1) is implemented as a parallel connection of all five FB resistors in fig. 4.2. When the first threshold is reached the switch in the outermost branch is opened and the remaining four branches form the resistive FB for which the second lowest gain value (1.26) is achieved. This pattern is then followed throughout the rise of the input signal until the maximum gain (2.85) configuration, where all switches are open and only the innermost branch is active. As the signal amplitude begins to fall the same behavior is observed in reverse.

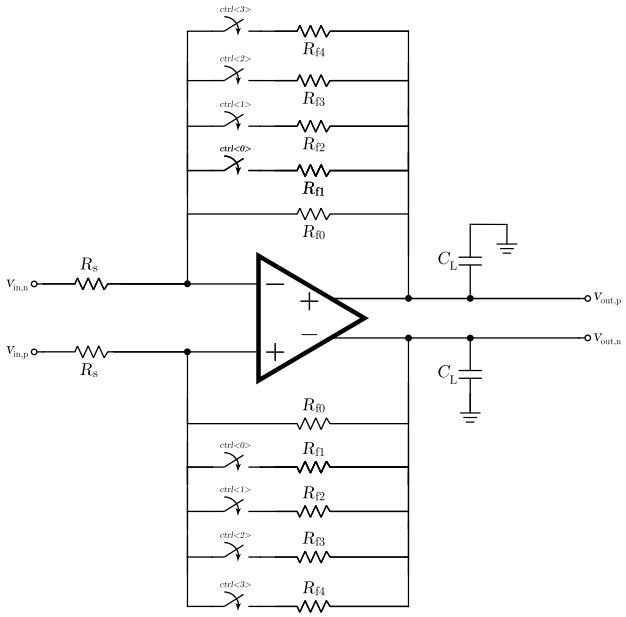
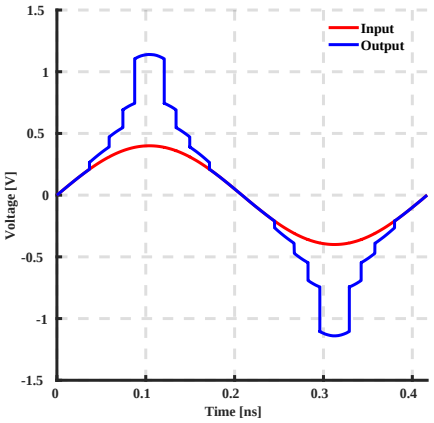
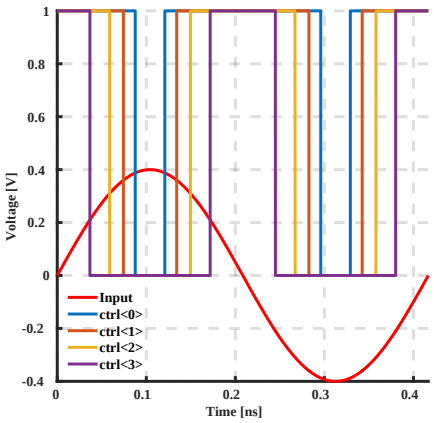


Figure 4.2: Schematic depicting switched FB network applied to Op-Amp



(a) Input and output signal for switched FB applied to ideal Op-Amp model



(b) Input signal and switch control signals for FB network

Figure 4.3: Waveforms demonstrating switched resistive FB for sinusoidal input signal

Figures 4.3a and 4.3b show a comparison between the input and output waveform as well as the switch control signals generated by the external source.

CMOS switches

When considering the implementation of switches in CMOS, the most straight forward answer may seem to be the use of a simple transistor with a control signal at its gate, serving to either pass or block a signal across its source and drain terminals. This however, has the significant drawback of limited signal swing for which the switch operates as intended [13].

The signal swing which the transistor is capable of accommodating will depend on if the device used is a PMOS or NMOS. For NMOS switches the output will have an upper bound of $V_{OUT,max} = V_{DD} - V_{thn}$ whereas for PMOS switches the limit is at the lower end with $V_{OUT,min} = |V_{thp}|$ (V_{thn} and V_{thp} are the respective threshold voltages for NMOS and PMOS) [13].

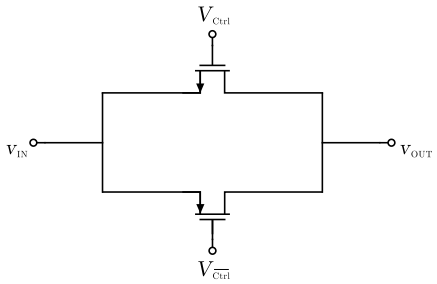


Figure 4.4: Complementary PMOS and NMOS switch

Figure 4.4 shows a method of resolving this issue by the use of a complementary PMOS and NMOS switch known as a transmission gate switch. Such an implementation allows for proper operation for rail-to-rail signals with the NMOS operation dominating at the lower end and PMOS at the higher.

The transmission gate switch may be equated to a series RC connection and a central consideration when designing these switches is to size the devices in such a way that the equivalent resistance of the switch (R_{eq}) demonstrates minimal variation with the input range [13]. Furthermore, a significant quantity is the total equivalent capacitance (C_{eq}). There is typically a tradeoff between minimizing the alterations in R_{eq} and the total value C_{eq} as larger devices demonstrate lower resistance at the cost of increased intrinsic capacitance values. The design of such a switch revolves mainly around finding the optimal balance of these parameters for the intended application.

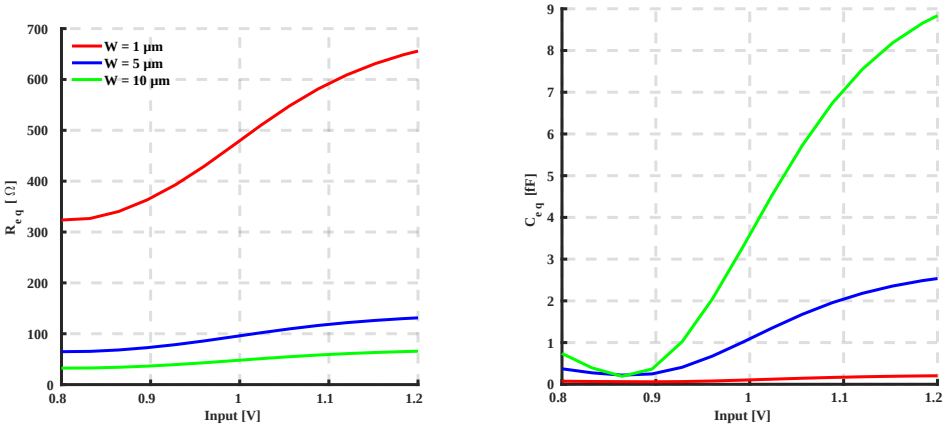
4.1.2 CMOS Switch Characterization

For the switched resistive FB network in this work, transmission gates were selected as the implementation of the switches intended for use in the circuit. As explained in section 4.1.1, the tradeoff between R_{eq} and C_{eq} was taken into consideration for the design.

$$R_{eq} = -\frac{1}{Re\{Y_{12}\}} \tag{4.3}$$

$$C_{eq} = \frac{Im\{Y_{12}\}}{2\pi f} \tag{4.4}$$

The values for these quantities were determined from S-parameter analyses of the transmission gate as a two-port network by observing the real and imaginary components of the Reverse Transfer Admittance Parameter (Y_{12}) across an input voltage sweep. Equations (4.3) and (4.4) show the respective expressions used to derive R_{eq} and C_{eq} from two-port simulation results.



(a) R_{eq} plotted against input sweep

(b) C_{eq} plotted against input sweep

Figure 4.5: R_{eq} and C_{eq} from transmission gate simulations for different transistor sizes

Figures 4.5a and 4.5b show the R_{eq} and C_{eq} plotted against input voltage for a transmission gate switch at different device sizes (PMOS to NMOS ratio is 1:1). As the input CM voltage was selected to be $1\,V$ in section 3.3.1 and the single-ended signal swing is specified as $0.4\,V_{PP}$ the input is swept from $0.8\,V$ to $1.2\,V$. It may be observed that the R_{eq} varies less as the transistor sizes are increased which comes at the cost of an increased C_{eq}. Furthermore, the minima in both plots occur close to $0.8\,V$ at the switch input which is due to the DC level at the switch output being set to the $0.8\,V$ selected as the CM output level of the Op-Amp in section 3.3.

Observing the effects of the tradeoff between R_{eq} and C_{eq} directly when applied to the Op-Amp and FB network was deemed more efficient rather than relying on assumptions derived beforehand. Therefore, sizes for the switches in the final design will be set based on simulation results in section 4.1.4.

4.1.3 Determining Resistor Values

As a starting point the R_{eq} which would be introduced by connecting the switches in series with the FB resistors was ignored as well as any gain error caused by the limited OL gain of the Op-Amp. With these assumptions made the approximation in eq. (4.2) may be used to determine the ratio of the total resistance in the FB (R_f) and the series resistance connected at the input terminals (R_s) seen in fig. 4.2.

$$R_{f0} = G_{max} R_s \tag{4.5}$$

$$R_{fk} = \frac{G_{5-k} R_s}{1 - G_{5-k} R_s \sum_{i=0}^{k-1} \frac{1}{R_{fi}}} ; \quad k = [1, 4] \tag{4.6}$$

$$\frac{R_{fk}}{R_s} = \frac{G_{5-k}}{1 - G_{5-k} \sum_{i=0}^{3} (\frac{R_{fi}}{R_s})^{-1}} ; \quad k = [1, 4] \tag{4.7}$$

The R_s was selected as $500\,\Omega$ as this value yielded the best results in simulations. Combining eqs. (4.5) and (4.6) results in eq. (4.7), allowing for the ratio of each individual resistor (R_{fk}) in the FB network and Rs to be determined according to the desired gain (G_{5-k}) specified in table 2.1. Table 4.1 shows the initial ratios of FB resistors to R_s obtained as a starting point before simulation.

FB Resistor	**Value**
R_{f0}	$2.85R_s$
R_{f1}	$5.88R_s$
R_{f2}	$7.3R_s$
R_{f3}	$7.37R_s$
R_{f4}	$4.85R_s$

Table 4.1: Table of initial FB resistor ratios to input series resistor

4.1.4 Switched Resistive FB Simulation and Tuning

The simulations for the FB network in this section were done applied to the RC and indirectly compensated Op-Amps separately. Initial simulations are run at a low frequency ($100\,MHz$) to remove any distortions caused by the limited performance of the amplifiers discussed in section 3.3.2. This is done for the sake of properly evaluating the functionality of the switched FB network. The maximum frequencies for which the circuits demonstrate proper behavior, with clearly visible steps in the output waveform, as seen for the ideal model in fig. 4.3a are then subsequently discussed. These steps are an indication that the amplifier is able to settle in time to properly keep up with the gain transitions and their appearance in the output characteristic is used as a measure of the Op-Amp being "fast enough".

Switches were set to use the minimum size for transistors ($\frac{W}{L} = \frac{1\,\mu m}{20\,nm}$) as this was determined to give the best results from simulations. The reason being that, as will be seen later in this section, the main limiting factor for the design is the shift in phase between input and output, which is only exacerbated by the introduction of additional capacitances to the circuit. Therefore, reduction of the C_{eq} of the switches becomes the more significant concern. Aditionally, $500\,\Omega$ resistors were applied to the gates of the MOSFETs used in the switch to prevent signal leakage into these terminals during operation (as the parasitic capacitances between the gate and drain/source nodes become low impedance connections at higher frequencies). A schematic for the implemented transmission gate switches is shown in fig. 4.6.

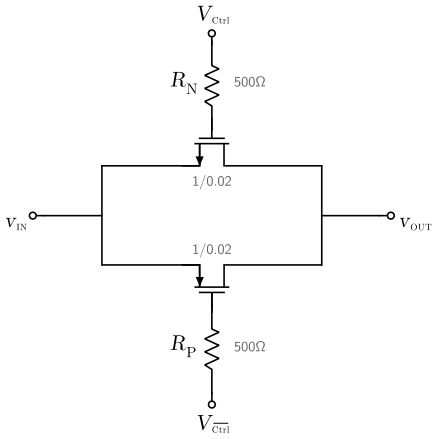


Figure 4.6: Schematic depicting CMOS switch implementation used in the final design

The switch control signals are generated by an ideal component modeled in verilogA following the characteristic shown in fig. 4.3b.

Simulation with the RC Compensated Op-Amp

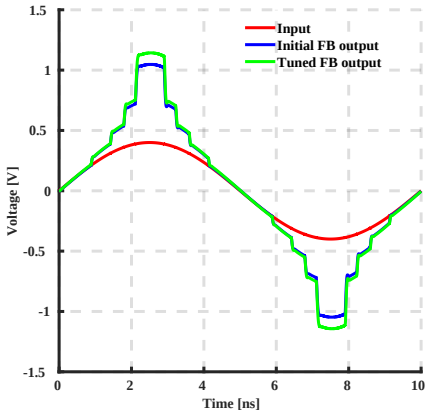


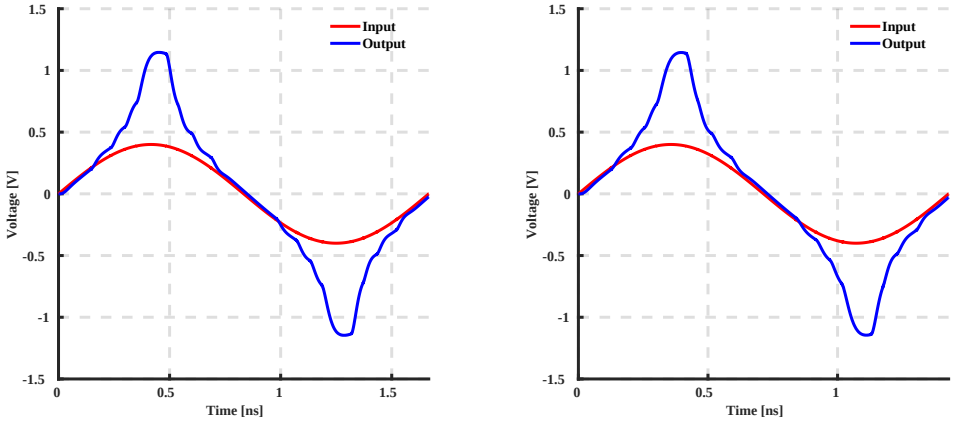
Figure 4.7: Input and output transient waveforms for switched resistive FB network applied to RC compensated Op-Amp at $100MHz$

Simulating the initial switched FB network from table 4.1 with the RC compensated Op-Amp at $100\,MHz$, the shape of the output waveform is as expected however the gain values are incorrect and the resistor ratios were therefore tuned to get the desired behavior for the circuit. Figure 4.7 shows a comparison of the waveforms for the initial and the tuned resistive FB achieving the correct gain values. The new resistor ratios are given in table 4.2.

With the FB network properly configured, a sweep is run to evaluate the maximum

FB Resistor	Value
R_{f0}	$2.85R_s$
R_{f1}	$5.88R_s$
R_{f2}	$7.3R_s$
R_{f3}	$7.37R_s$
R_{f4}	$4.85R_s$

Table 4.2: Table of FB resistor ratios to input series resistor after tuning



(a) Simulation at $600\,MHz$, still showing discernible steps

(b) Simulation at $700\,MHz$, steps start becoming unclear

Figure 4.8: Frequency sweep for switched resistive FB applied to RC compensated Op-Amp

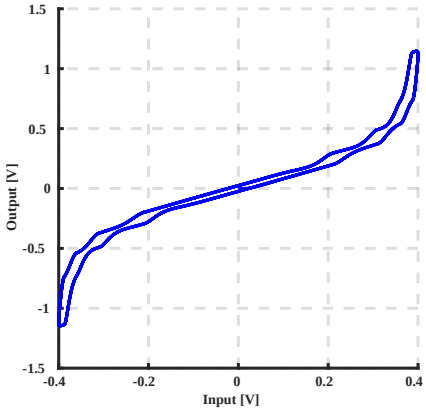
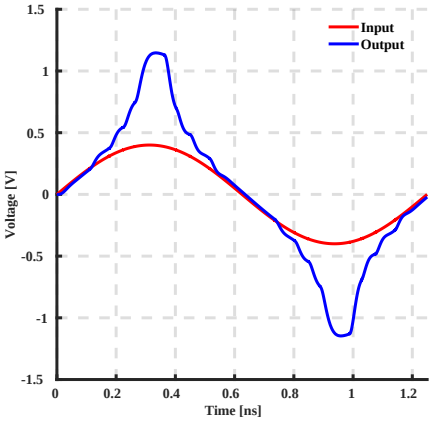


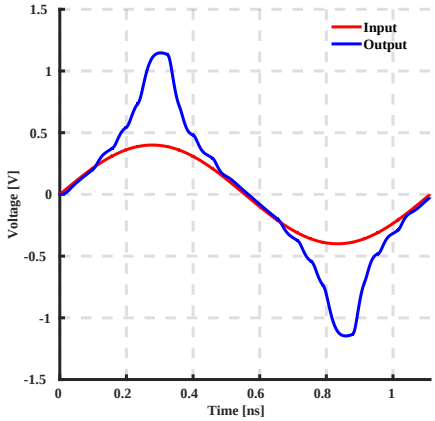
Figure 4.9: Transfer characteristic of switched FB applied to RC compensated Op-Amp at $600\,MHz$ (simulation for 5 signal periods)

frequency at which the circuit performs as desired. Figure 4.8a shows the input and output waveforms for at $600\,MHz$ with the steps in between gain transitions still clearly visible. As a comparison fig. 4.8b illustrates how at $700\,MHz$ the steps become unclear and the functionality of the circuit is compromised. Furthermore, it may be observed that the falling and rising output transitions are asymmetrical. This causes the "gap" in the transfer characteristic seen in fig. 4.9, another major limitation in the design. This is caused by the phase shift between the Op-Amp input and output discussed in section 3.3. Since the switch control signal is generated based on the times at which the input amplitude reaches each breakpoint threshold, these points become asymmetrical in the output waveform as it is delayed in time by the phase shift.

Simulation with the Indirectly Compensated Op-Amp



(a) Simulation at $800\,MHz$, still showing discernible steps



(b) Simulation at $900\,MHz$, steps start becoming unclear

Figure 4.10: Frequency sweep for switched resistive FB applied to Indirectly compensated Op-Amp

When simulating the indirectly compensated Op-Amp with the resistor values from table 4.2 the gain values were found to be correct and thus no further tuning was deemed necessary. Observing the transient waveforms in figs. 4.10a and 4.10b it may be seen that the indirect compensation demonstrates an overall improvement in terms of speed, the frequency at which the circuit fails now being $900\,MHz$, a $200\,MHz$ improvement when compared with the RC compensation. $800\,MHz$ was deemed to be the performance limit for the indirectly compensated design. The gap in the transfer characteristic is still visible in fig. 4.11 and is again caused by the phase shift between the input and output.

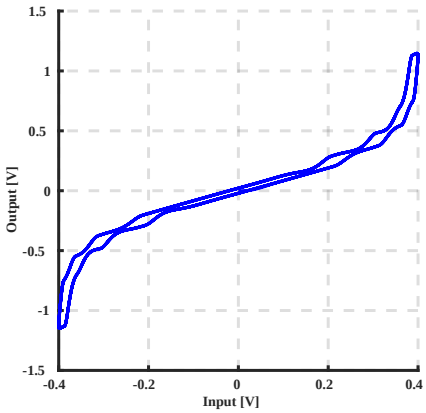


Figure 4.11: Transfer characteristic of switched FB applied to indirectly compensated Op-Amp at $800\,MHz$ (simulation for 5 signal periods)

4.2 Current Injection Scheme Design and Simulation Results

From comparing the two Op-Amps in section 4.1 the indirectly compensated design exhibits an overall superior performance. All simulations in this section are therefore done with the indirectly compensated Op-Amp.

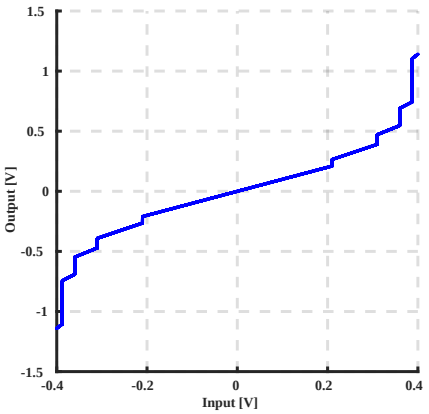
4.2.1 Conceptual Background

In chapter 2 it was briefly alluded to the fact that even with an ideal Op-Amp the transfer characteristic would not match the desired gain expansion function. The actual result from only applying a switched resistive FB would, even in the ideal case, consist of discrete steps at the breakpoints rather than the smooth linear transitions required to realize a piecewise linear behavior.

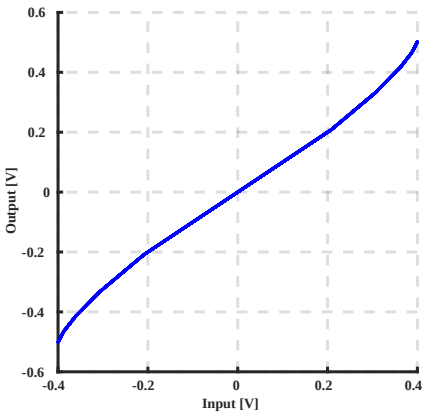
From fig. 4.3a it may be observed that at each switching point the output waveform exhibits a jump as the amplifier abruptly switches between gain regimes, reflected by the steps seen in the transfer characteristic in fig. 4.12a. This suggests the need for some sort of technique to smoothen out these transitions, making the gain switching gradual rather than an abrupt transition. Figure 4.12b shows the transfer characteristic of this proposed current injection applied to an ideal Op-Amp model. As may be observed, the characteristic is now smoothed out and the abrupt jumps are removed, ensuring the correct piecewise linear behavior.

4.2.2 Current Injection Scheme Implementation

Due to time constraints, a realistic implementation for the current injection scheme was not explored during the course of this thesis. Rather, it was decided to leave the actual realization of a current injection system to future work and the focus for this work was



(a) No current injection, transfer characteristic exhibits abrupt jumps



(b) Current injection, transfer characteristic is smoothed

Figure 4.12: Transfer characteristic of switched FB without and with current injection applied to ideal Op-Amp (simulation for 5 signal periods)

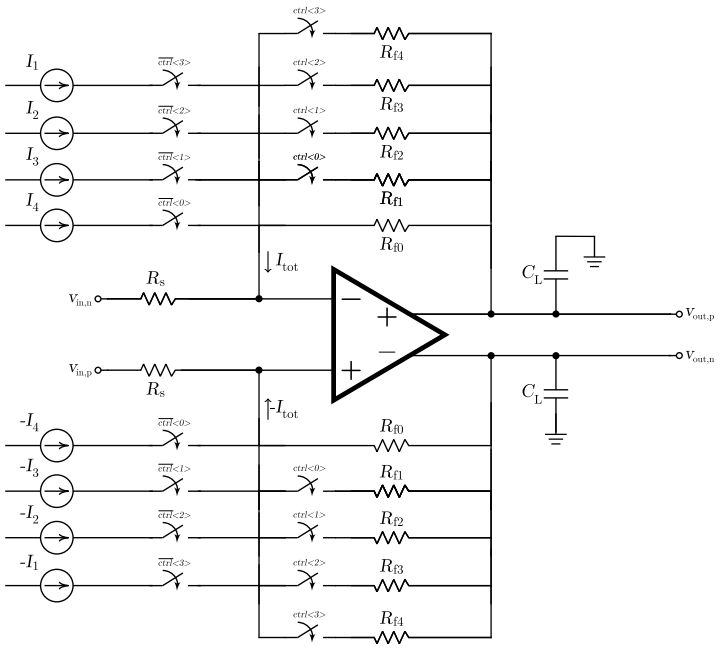
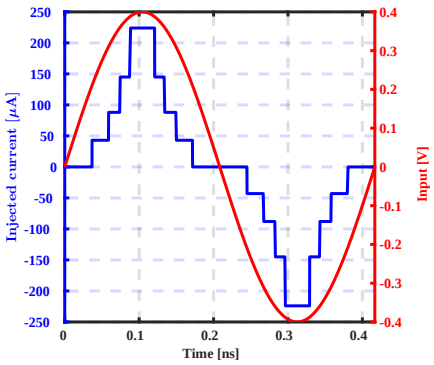


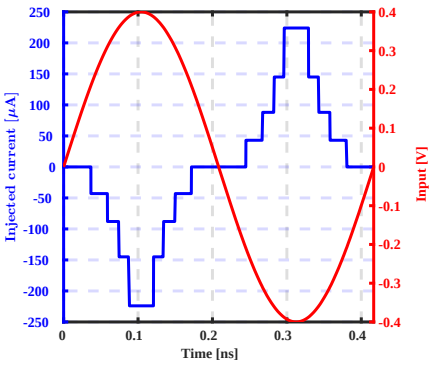
Figure 4.13: Schematic depicting concept behind current injection scheme

a conceptual evaluation of such a system. The schematic in fig. 4.13 shows the intended behavior for this component. The control follows the opposite signals of the FB switches. As each switch is opened, a new current is injected (the sum of all the currents in the

now active branches equaling I_{tot}). For example at the minimum gain, with all branches closed, there is no current and for the maximum gain when all FB switches are open, the injected current reaches its peak value of $I_{tot} = I_1 + I_2 + I_3 + I_4$.



(a) Comparison of injected current for the upper side with input



(b) Comparison of injected current for the lower side with input

Figure 4.14: Injected currents from verilogA component compared with differential input waveform

The current injection itself was modeled as an ideal component using verilogA. The functionality of this model is illustrated in figs. 4.14a and 4.14b. Opposite currents are injected for the upper (fig. 4.14a) and lower (fig. 4.14b) branches seen in fig. 4.13 since the single-ended signals are of opposing polarities.

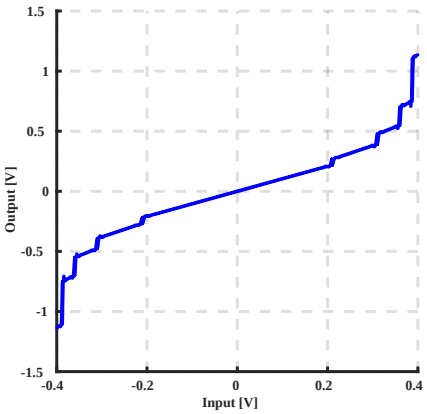
Table 4.3 provides the values for signal amplitudes at each breakpoint as well as the respective total injected currents following.

Input Signal Amplitude [V]	**Total Injected Current [μA]**
0	-
0.21	38
0.31	85
0.36	143
0.3875	222

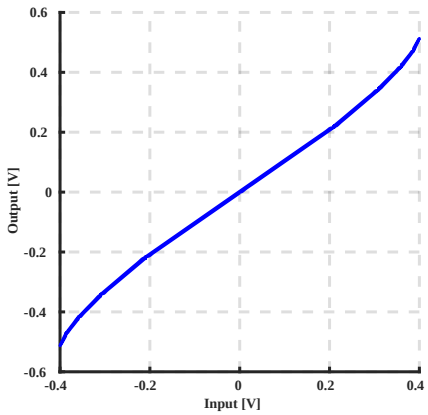
Table 4.3: Table showing breakpoints and injected currents

4.2.3 Simulation Results

Shown in fig. 4.15b is the resulting transfer characteristic from applying the current injection to the switched resistive FB with the indirectly compensated Op-Amp at $100\,MHz$ input frequency. Figure 4.15a shows the same without current injection for comparison. As expected the abrupt jumps are removed while the correct slope following each breakpoint is retained and the output amplitude is reduced. Figure 4.16 depicts the transient input and output waveforms with current injection as well as without at this



(a) No current injection, transfer characteristic exhibits abrupt jumps



(b) Current injection, transfer characteristic is smoothed

Figure 4.15: Transfer characteristic of switched FB without and with current injection applied to indirectly compensated Op-Amp at $100\,MHz$ (simulation for 5 signal periods)

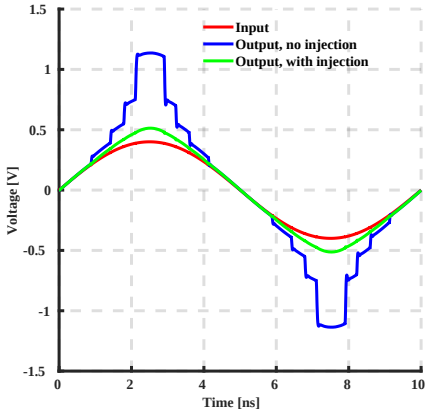
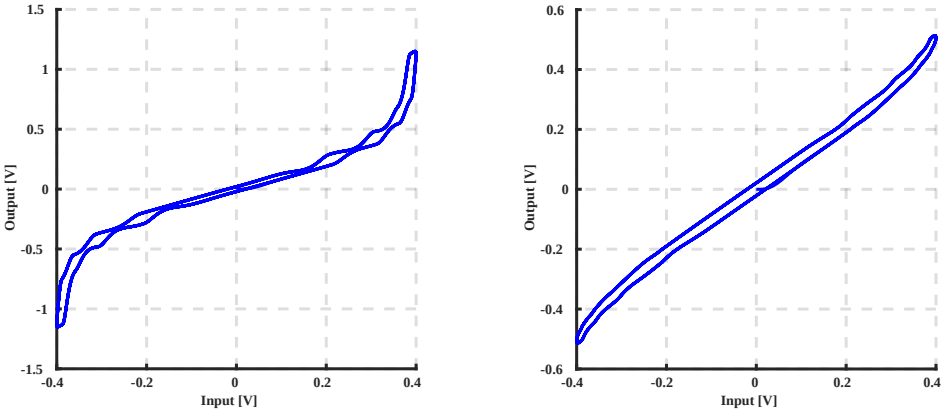


Figure 4.16: Transient waveforms for current injection applied to indirectly compensated Op-Amp at $100\,MHz$

same frequency. There are no visible steps in the output response now, but the amplitude is pushed down by the injected currents.

Further evaluation is now done for higher input signal frequencies. From figs. 4.17a and 4.17b, depicting the transfer characteristics at $800\,MHz$, it may be noted that the gap, caused by the phase shift between the input and output of the circuit discussed in section 4.1.4, remains the main limitation for the design. Figure 4.18 shows the transient input and output waveforms at this input frequency for comparison.



(a) No current injection, transfer characteristic exhibits abrupt jumps

(b) Current injection, transfer characteristic is smoothed

Figure 4.17: Transfer characteristic of switched FB without and with current injection applied to indirectly compensated Op-Amp at $800\,MHz$ (simulation for 5 signal periods)

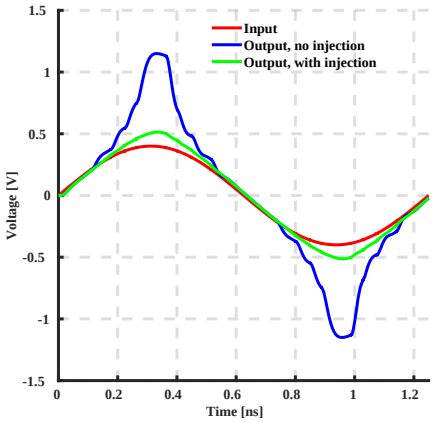


Figure 4.18: Transient waveforms for current injection applied to indirectly compensated Op-Amp at $800\,MHz$

Chapter 5
Conclusion

This thesis proposes baseband analog pre-distortion, serving to linearize out of band IM3 components in a combined DPD and APD system for mm-W PAs. The main advantage of such a solution being independence of the PA topology an operating frequency. Furthermore, a piecewise linear gain expansion was set as the target for the transfer function, enabling tunability and allowing for the system to be applicable to PAs with various distortion profiles. The thesis scope covers the design of the core block for this APD system, realizing the aforementioned transfer function. The block consists of an Op-Amp with a switched resistive FB network.

Initially the system was evaluated from a theoretical point of view by verifying the concepts behind the design through the use of ideal models. These results were then characterized, setting the performance specifications for the Op-Amp and the complete design seen in table 2.2.

At first, the Op-Amp was designed and evaluated stand-alone. The selected topology ended up being a two stage fully differential amplifier. Two stages were deemed necessary to handle the voltage swings required as per the results from the initial theoretical modeling. Originally, the frequency compensation for the Op-Amp was implemented with a miller capacitance and a zero-nulling resistor. The main limitation in the performance of the circuit was found to be its inability to accommodate the specified $2.4\,GHz$ maximum input signal frequency. The limiting factor was found to be in the phase response as the design did meet the specification for the GBW from table 2.2 but a phase delay between the input and output is present. For this reason, an alternative frequency compensation was explored, using a buffer connected to feed the current through the compensation capacitance to the output of the first stage. The method was shown to present a notable reduction in the phase shift (a reduction from -25.2° to -16.9° at $2.4\,GHz$). However, the performance improvement exhibited by the alternative compensation comes at the cost of increased overall power consumption for the amplifier ($41.68\,mW$ as opposed to the $27.824\,mW$ of the RC compensated design), deemed an acceptable tradeoff.

Following the design of the Op-Amp a switched resistive FB network was implemented, enabling the dynamic control of the circuit gain by an external system. As a result the output characteristic may be divided into sections, each with a different gain value, resulting in regions of alternating slopes in the transfer function. To achieve the desired piecewise linear form, an additional step was needed, namely the introduction of a current injection scheme which would remove the abrupt jumps between these regions. Due to time constraints, proper implementation for the current injection was not explored

in this work and the functionality was instead modeled ideally as a verilogA component. Results with the ideal model confirm the validity of this idea as the circuits transfer function now follows the intended piecewise linear form.

Table 5.1 shows a comparison between the target specifications and those achieved by the final design.

Performance Specification	**Target**	**Achieved value**
Maximum signal BW	$1.6\,GHz$	$533\,MHz$
Slew rate	$8.6\,V/ns$	$28.6\,V/ns$
DC power consumption	$35\,mW$	$41.68\,mW$

Table 5.1: Table showing comparison between target specifications and those achieved by the design

Overall, the main limitation for the circuit designed in this thesis was determined to be the appearance of a phase delay at higher frequencies, making it unable to support the originally intended $2.4\,GHz$ BW. This specification was based on the assumption for a worst case $1.6\,GHz$ input signal BW to the APD system, resulting in a $800\,MHz$ BW for the I/Q components. Since the APD is meant to linearize IM3 distortions it must cover 3 times the I/Q BWs, hence the $2.4\,GHz$ specification. The maximum frequency for which the design behaves acceptably was found to be $800\,MHz$, meaning the system would be able to handle a third of the worst case BW ($533\,MHz$). This suggests the need for future work to be done to mitigate the issue by either exploring different amplifier topologies or a possible mechanism in the FB network which would compensate the phase shift (i.e. accounting for the phase delay in the generation of the switch control signals).

As for the SR target, it was greatly exceeded. However, the target SR was calculated based on a $2.4\,GHz$ sinusoidal input signal with the maximum gain but the actual limit in terms of speed for the circuit would be defined by the time and gain difference between two adjacent breakpoints. This may require a greater slew rate for the amplifier to settle in time and the consequence can be seen in the output waveforms discussed in section 4.1.4.

Although the indirect frequency compensation resulted in an improved performance, it may be noted that it significantly increases the power consumption, exceeding the $35\,mW$ target specified by internal investigations at Ericsson.

Appendices

Appendix A

Fixing Gain in Smoothed Transfer Function

In section 4.2 it may be noted that injecting current to smooth out the output waveform retains the original slopes in the function, but the actual output amplitude of the circuit is reduced. If keeping the output amplitude is also a consideration the design would have to be modified as the slopes following each breakpoint would need to be made sharper to i.e. the gain following each point must be increased. Furthermore, the original design where the switched feedback scales the gain through connecting active branches in parallel. This makes each value for gain dependent on the configuration used to achieve the preceding value and such interdependence causes resistor values to become extreme for achieving more drastic differences in adjacent slopes, especially for the designed five breakpoints.

An alternative implementation for the switched feedback network was therefore explored following the completion of the project. This appendix will briefly explain the changes made in section A.1 and section A.2 will present the new simulation results.

A.1 Switched Feedback Network Redesign

Seen in fig. A.1 is a schematic showing the concept behind the new FB network and current injection scheme. The switches now only close one at a time such that only a single branch is active at any given moment. This way, the circuit gain is defined by only one branch at a time. Figure A.2 shows the new switch control signals compared to the differential input waveform. Now the innermost branch defines the lowest gain value and the outermost defines the maximum and currents are injected one at a time such that $I_{tot,min} = 0$ and $I_{tot,max} = I_4$.

Also, the slope values would have to be increased compared with the original design for the smoothed piecewise linear transfer characteristic to reach the same maximum amplitude as that without current injection. Drastically so, for the slope following the final breakpoint. Initial testing showed that after the final point the amplifier was not able to slew fast enough to achieve the maximum amplitude at this high gain and therefore all breakpoints were moved down by $50\,mV$ compared to those in table 2.1. Table A.1 provides the values for the reconfigured breakpoints and FB branch resistor values as well as the currents injected following each point.

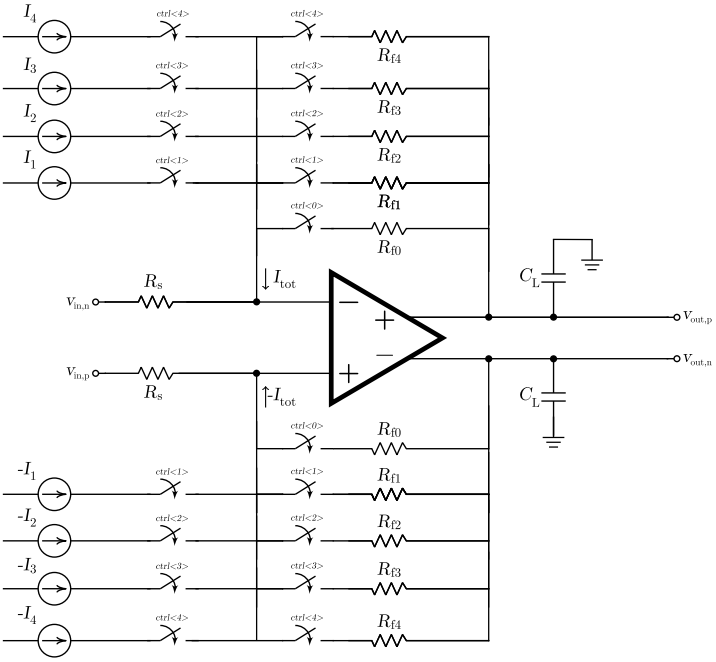


Figure A.1: Schematic depicting concept behind modified current injection scheme

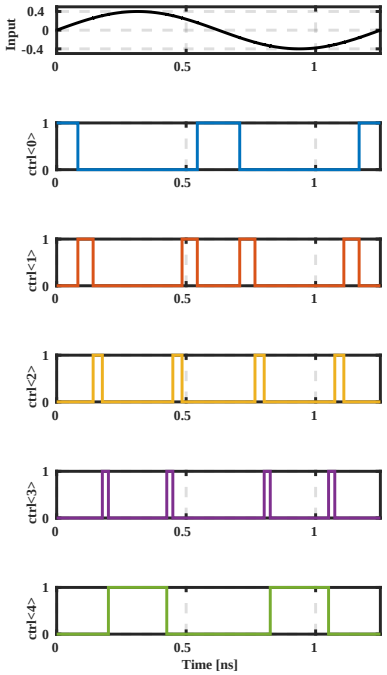
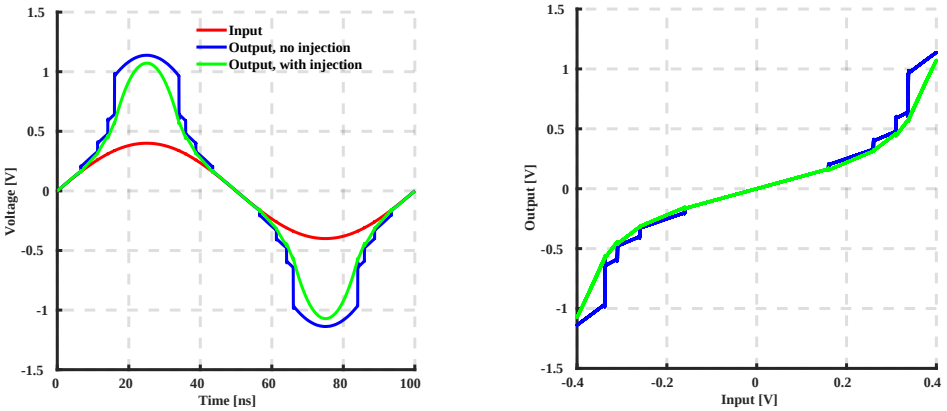


Figure A.2: Modified switch control signals and differential input

Input Signal Amplitude [V]	Branch FB Resistor	Injected Current [μA]
0	$R_{f0} = 0.4R_s$	-
0.16	$R_{f1} = R_s$	60
0.26	$R_{f2} = 2.5R_s$	150
0.31	$R_{f3} = 5R_s$	220
0.3375	$R_{f4} = 10R_s$	270

Table A.1: Table showing reconfigured breakpoints, feedback resistor vales and injected currents

A.2 Simulation Results



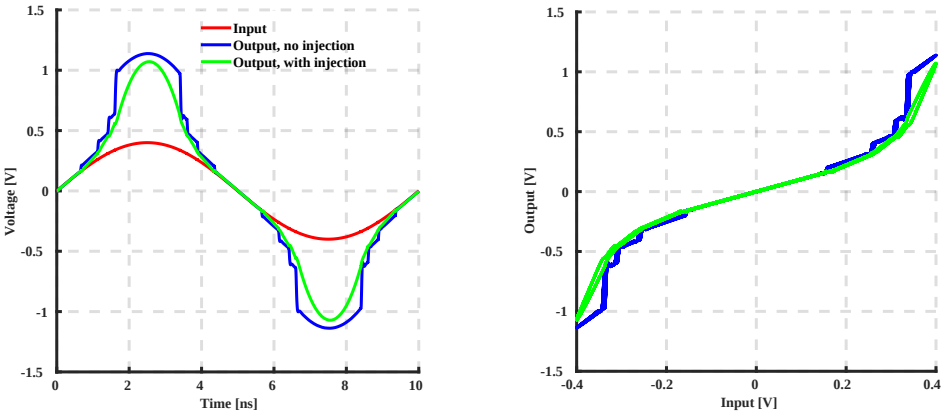
(a) Transient waveforms compared

(b) Transfer characteristic compared

Figure A.3: Transient waveforms and transfer characteristics compared with and without current injection at $10\,MHz$

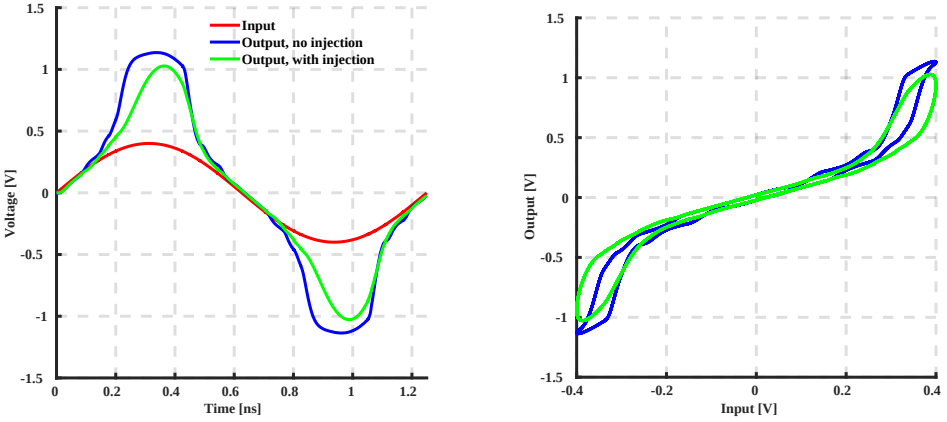
At first, the circuit behavior is evaluated at low frequencies. Figures A.3a and A.3b show comparisons of the transient waveforms and transfer characteristics for the modified circuit at $10\,MHz$ input signal frequency respectively. As can be noted, the maximum output amplitude is now very close to that observed without any current injection, confirming the validity of this approach.

Figures A.4 and A.5 show comparisons at $100\,MHz$ and $800\,MHz$. At $100\,MHz$ a slight gap may be observed following the final brakpoint in the smoothed transfer characteristic, becoming more pronounced at $800\,MHz$. This shows that at higher gain values the circuit struggles to keep up with the switching. Further investigation is needed here and is left for future work.



(a) Transient waveforms compared **(b)** Transfer characteristic compared

Figure A.4: Transient waveforms and transfer characteristics compared with and without current injection at $100\,MHz$



(a) Transient waveforms compared **(b)** Transfer characteristic compared

Figure A.5: Transient waveforms and transfer characteristics compared with and without current injection at $800\,MHz$

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